

Key Features

- **Industry first** ultra-high performance AMC-module with multi-core DSP, high-capacity FPGA and FMC site for modular MicroTCA® and AdvancedTCA® DSP systems and stand-alone embedded applications
- Installs into MicroTCA® chassis and AdvancedTCA® mainboards
- FMC site for user application adopted I/O (AD/DA, SFP+, QSFP+, SDR, RF, etc.) using FMC submodule
- In-chassis AMC-to-AMC high-speed real-time data transfer via AMC interface using 10GbE/40GbE, Serial RapidIO and PCIe protocols
- High-speed multi-channel DSP-to-FPGA communication
- Remote control from host PC and Android® devices and in-chassis AMC-to-AMC control via AMC 1GbE ports
- Unified **TASDK®** tools for application development and system control
- Complies with PICMG® 3.0 Rev.3.0, MicroTCA.0 R1.0, AMC.0 R2.0, IPMI 1.5, VITA® 57.1-2008 specifications
- Stand-alone operation from +12V power for embedded applications

Details

- 8-core TI TMS320C6678 DSP (1.25GHz 320GMAC/160GFLOPS)
- Xilinx Virtex-7 FPGA (XC7VX330T, XC7VX415T, XC7VX690T)
- VITA® 57.1 FMC HPC site for FMC submodule (160 I/O, 8 GBTs)
- AMC Fabric-D/E/F/G ports 4-7 and 8-11 with FPGA transceivers comply 10GbE, 10GBASE-BX4, 40GBASE-CX4, 4x Serial RapidIO (39.4Gbps), 4x PCIe (32Gbps) protocols
- AMC 1GbE Fabric-A 0-1 ports with DSP transceivers for remote control and in-chassis AMC-to-AMC control communication
- DSP-to-FPGA communication via 4x Serial RapidIO ports (40Gbps bidirectional bandwidth), EMIF-16 interface and DSP GPIO/IRQ
- Up to 8GB of DSP DDR3 memory
- 1Gb NOR FLASH for DSP bootloader, system monitor, applications, data arrays and FPGA bitstreams with file system support
- Nonvolatile 128KB MRAM memory for critical DSP application data
- x64 (up to 8GB) and x32 (up to 4GB) FPGA DDR3 memory banks
- DSP and MMC UART ports for remote control and management
- Front-panel DSP and FPGA user application controlled LEDs
- JTAG ports for DSP, FPGA and FMC site
- MMC controller based on MicroLAB Systems propriety **TAMMC®** high-speed MMC-kernel with monitoring of power supplies and temperatures and status indication for reliable device operation and protection

Development Tools

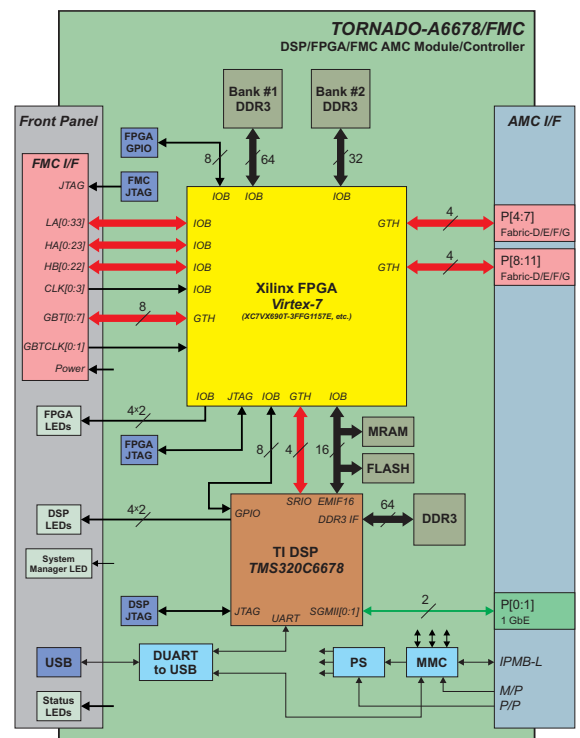
- TI *Code Composer Studio* tools and MicroLAB Systems **MIRAGE-NE1** JTAG emulators to compile and debug user DSP applications
- Xilinx *ISE/Vivado* tools and IP to compile and debug user FPGA firmware
- Unified **TASDK®** tools with high-level API, bootloader and system monitor to quickly design cross-platform user DSP applications and host Windows, Linux and Android® applications for all **TORNADO-Axxx** AMC-modules
- DSP and FPGA demos for device tests and user design startup

Applications

- Telecommunication and cell telephony
- RF and SDR
- Image processing
- Radars and astrophysics
- Industrial, instrumentation and medical



[TORNADO-A6678/FMC](#) AMC Module (M/S)



[TORNADO-A6678/FMC](#) Block Diagram



Mini TORNADO-mMTCA® DSP/FPGA modular system with [TORNADO-A6678/FMC](#) DSP/FPGA/FMC M/S AMC-module and [TAX-DSPX](#) network AMC-module in dual-slot MicroTCA® mini chassis with passive backplane

Technical Specifications (*TORNADO-A6678/FMC rev.1B*)

DSP

- Texas Instruments TMS320C6678 Fixed/Floating-point DSP, 8-cores, 1.25GHz (320GMAC/160GFLOPS).
- 128M/256M/512M/1Gx64 (1GB/2GB/4GB/8GB) 1333MTPS on-board DDR3 memory (is specified on ordering).
- On-board 64Mx16 (1Gb) NOR FLASH with hardware/software write protection, non-volatile 128Kx8 MRAM memory with software write protection (optional, is specified on ordering), and 64Kx8 (512Kb) I2C EEPROM (optional, is specified on ordering).
- 4x 5Gbps Serial RapidIO ports (connected to FPGA transceivers).
- 2x 1GbE SGMII ports (connected to AMC I/F ports 0 and 1).
- 115kBaud UART port (available via USB port at front panel).
- EMIF-16 16D/24A I/F (used to access FLASH, MRAM, user FPGA on-chip logic, etc).
- DSP Bootmodes: None/Debug, EMIF/FLASH, Ethernet.
- Debug port: TI JTAG (14-pin, LVTTTL 3V) via adapter cable.

FPGA

- Xilinx Virtex-7: XC7VX330T-[2/3]FFG1157[C/E/I], XC7VX415T-[2/3]FFG1157[C/E/I], XC7VX690T-[2/3]FFG1157[C/E/I].
Options to specify on ordering: FPGA type, speed grade ([-2/-3]), temperature index ([C/E/I]).
Default FPGA is XC7VX415T-2FFG1157C.
- Two on-board FPGA DDR3 memory banks (optional, are specified on ordering):
 - Bank #1: 128M/256M/512M/1Gx64 (1GB/2GB/4GB/8GB)
 - Bank #1: 128M/256M/512M/1Gx32 (512MB/1GB/2GB/4GB)
- 8-bit external FPGA GPIO[0:7] (LVTTTL 3V) with individual IN/OUT control via FPGA.
- FPGA bitstream loading modes: from DSP applications, via JTAG.
- FPGA bitstream decryption key battery (optional, is specified on ordering). User replaceable every 5 years.
- Debug port: Xilinx JTAG (14-pin, LVTTTL 3V) via adapter cable.

FMP site interface

- Complies VITA 57.1-2008 specification.
- FMC mezzanine submodule width: single.
- FMC mezzanine submodule stacking: 10mm (default), 8.5mm (optional).
- FMC interface type: HPC, LPC.
- Number of I/O: 160 (LA[0:33], HA[0:23], HB[0:21]).
- Number of I/O clocks: 4 (CLK_M2C[0:3]).
- I/O logic levels (Vadj) for LA/HA/HB I/O pins and CLK_M2C clocks: 1.2V, 1.5V, 1.8V (is set automatically during activation of FMC submodule).
- Number of GBT transceivers: 8 (GBT[0:7]).
- GBT performance: 10.3Gbps (for FPGA with [-2] speed grade), 12.5Gbps (for FPGA with [-3] speed grade).
- Maximum FMC mezzanine submodule power consumption: 1A@+12V, 3A@+3.3V, 4A@Vadj, 50mA@+3.3V_AUX.
- Maximum FPGA FMC interface power consumption for FMC submodule provided power: 0.3A@VIO_B_M2C, 0.5mA@VREF_A_M2C, 0.5mA@VREF_B_M2C.
- Debug port: JTAG (10-pin, LVTTTL 3V) via adapter cable.

Front-panel

- A "window" for front bezel of FMC mezzanine submodule.
- User DSP application controlled LEDs: 4 (bi-color: Red/Green, Orange/Green, Green/Yellow, Red/Yellow).
- User FPGA firmware controlled LEDs: 4 (bi-color and tri-color: Red/Green, Orange/Green, Green/Yellow, Yellow/Green/Blue).
- AMC status LEDs: BLUE LED, AMC LED1 ("Power" function, Red/Green), AMC LED2 ("I^o" function, Yellow/Green).
- DSP Bootloader & System Manager Status LED (Yellow/Green/Blue).
- FPGA configuration status LED (Red/Green).
- FMC submodule status LED (Red/Green/Blue).
- Micro-USB port with MMC UART (115kBaude) and DSP UART (115kBaude).

AMC I/F

- Complies PICMG® AMC.0 R2.0, MicroTCA.0 R1.0 specifications.
- FPGA ports: AMC Fabric-D/E/F/G ports 4-7 and 8-11 (AMC.2 Ethernet, AMC.4 Serial RapidIO, AMC.1 PCIe).
- DSP ports: AMC-Fabric-A ports 0, 1 (AMC.2 1GbE).
- MMC ports: IPMB-L port

MMC module management controller

- Firmware based on high-performance [TAMMC®](#) MMC-kernel from MicroLAB Systems.
- Complies IPMI 1.5, IPMB CPS v1.0, PICMG® 3.0 rev.3.0, MicroTCA.0 R1.0, AMC.0 R2.0 and VITA® 57.1-2008 specifications.
- High-speed monitoring of payload power and all backend power supplies (voltage and current), tolerance control.
- Multi-point temperature monitoring of PCB, DSP and FPGA.
- Activation and status monitoring of FMC-submodule.
- Power and temperature status indication of AMC module and FMC-submodule via front-panel status LEDs and on-board LEDs.
- Remote MMC console via MMC UART 115kbaud port.

Physical

- Dimensions (is specified on ordering):
 - Single width Mid-size (M/S) AMC-module (181 x 74 x 19 mm) (default).
 - Single width Full-size (F/S) AMC-module (181 x 74 x 29 mm) (optional).
- Weight 0.35 kg.

Power and temperature

- AMC +12V P/P payload power or external +12V power for stand-alone embedded applications:
 - without FMC mezzanine module installed: +12V @ 2.5A (typ) (30W), 4A (max) (48W).
 - with max power FMC mezzanine module installed: +12V @ 3.4A (typ) (41W), 4.9A (max) (59W).
- AMC M/P management power: +3.3V @50mA (typ).
- Operating temperature (ambient) with 50CFM forced cooling: 0°C...+55°C.
- Storage temperature (ambient): -40°C...+80°C.

Ordering information

TA6678FMC1B/X415T2C/1.25G/D2/F1/E512/M128/F1D2/F2D1/FC/FB/SA/MS

TORNADO-A6678/FMC rev.1B AMC-module, Xilinx Virtex-7 XC7VX415T-2FFG1157C FPGA (**X415T2C**), 1.25GHz DSP clock frequency (**1.25G**), 2GB (256Mx64) DSP DDR3 memory (**D2**), 1Gb (64Mx16) DSP FLASH memory (**F1**), 512Kb (64Kx8) DSP I²C EEPROM memory (**E512**), 128Kx8 nonvolatile DSP MRAM memory (**M128**), 2GB (256Mx64) FPGA DDR3 memory bank #1 (**F1D2**), 1GB (256Mx32) FPGA DDR3 memory bank #2 (**F2D1**), FMC interface for FMC-submodule (**FC**), FPGA bitstream decryption key battery (**FB**), stand-alone mode support (**SA**), single-width mid-size (M/S) AMC-module dimension (**MS**), standard 10mm FMC mezzanine module stacking.