Mailbox Description 10

CONTENTS

Applied Micro Circuits Corporation
6195 Lusk Blvd., San Diego, CA 92121 • (619) 450-9333

10.0 MAILBOX OVERVIEW

The S5933 has eight 32-bit mailbox registers. The mailboxes are useful for passing command and status information between the Add-On and the PCI bus. The PCI interface has four incoming mailboxes (Add-On to PCI) and four outgoing mailboxes (PCI to Add-On). The Add-On interface has four incoming mailboxes (PCI to Add-On) and four outgoing mailboxes (Add-On to PCI). The PCI incoming and Add-On outgoing mailboxes are the same, internally. The Add-On incoming and PCI outgoing mailboxes are also the same, internally.

The mailbox status may be monitored in two ways. The PCI and Add-On interfaces each have a mailbox status register to indicate the empty/full status of bytes within the mailboxes. The mailboxes may also be configured to generate interrupts to the PCI and/or Add-On interface. One outgoing and one incoming mailbox on each interface can be configured to generate interrupts.

10.1 FUNCTIONAL DESCRIPTION

Figure 10-1 shows a block diagram of the PCI to Add-On mailbox registers. Add-On incoming mailbox read accesses pass through an output interlock latch. This prevents a PCI bus write to a PCI outgoing mailbox from corrupting data being read by the Add-On. Figure 10-2 shows a block diagram of the Add-On to PCI mailbox registers. PCI incoming mailbox reads also pass through an interlocking mechanism. This prevents an Add-On write to an outgoing mailbox from corrupting data being read by the PCI bus. The following sections describe the mailbox flag functionality and the mailbox interrupt capabilities.

Figure 10-1. Block Diagram - PCI to Add-On Mailbox Register

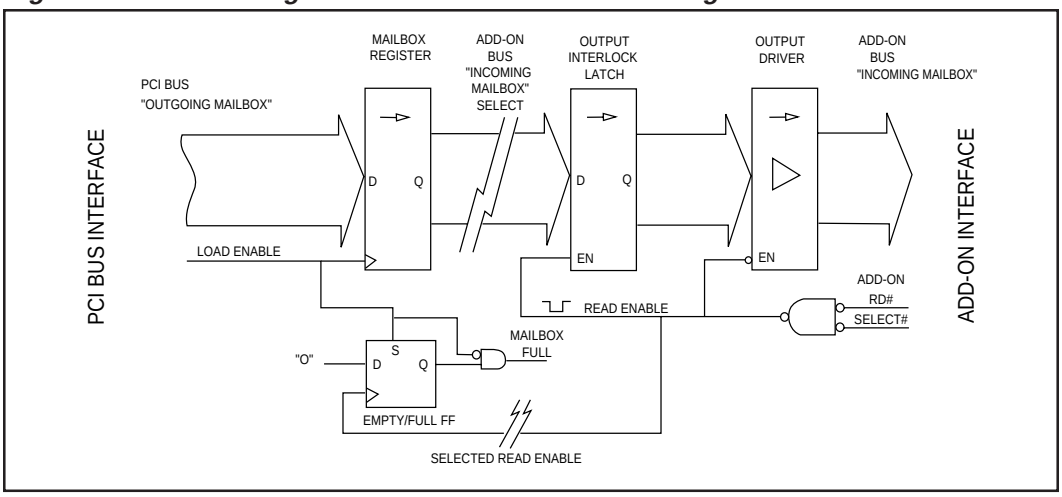
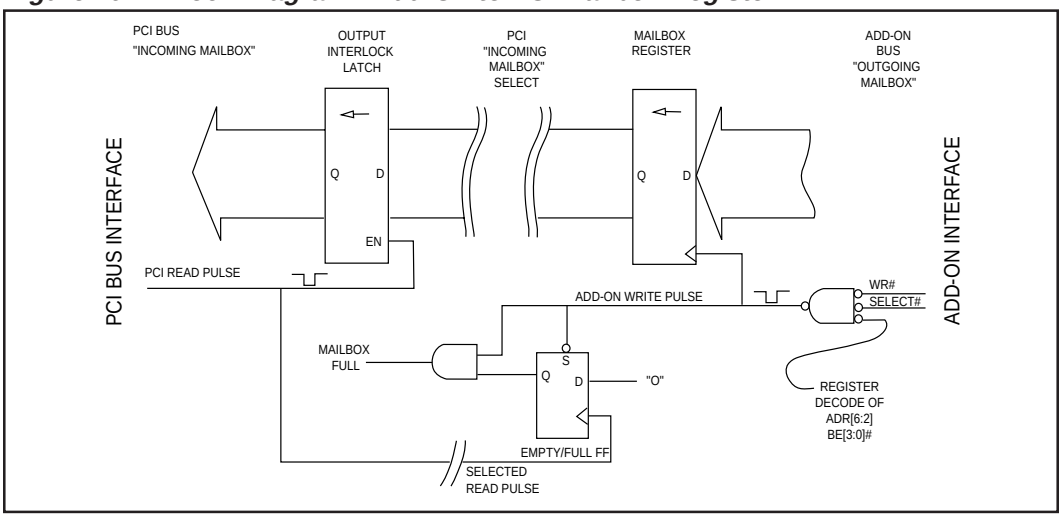


Figure 10-2. Block Diagram - Add-On to PCI Mailbox Register



10.1.1 Mailbox Empty/Full Conditions

The PCI and Add-On interfaces each have a mailbox status register. The PCI Mailbox Empty/Full Status (MBEF) and Add-On Mailbox Empty/Full Status (AMBEF) Registers indicate the status of all bytes within the mailbox registers. A write to an outgoing mailbox sets the status bits for that mailbox. The byte enables determine which bytes within the mailbox become full (and which status bits are set).

An outgoing mailbox for one interface is an incoming mailbox for the other. Therefore, incoming mailbox status bits on one interface are identical to the corresponding outgoing mailbox status bits on the other interface. The following list shows the relationship between the mailbox registers on the PCI and Add-On interfaces.

PCI Interface		Add-On Interface
Outgoing Mailbox 1	=	Incoming Mailbox 1
Outgoing Mailbox 2	=	Incoming Mailbox 2
Outgoing Mailbox 3	=	Incoming Mailbox 3
Outgoing Mailbox 4	=	Incoming Mailbox 4
Incoming Mailbox 1	=	Outgoing Mailbox 1
Incoming Mailbox 2	=	Outgoing Mailbox 2
Incoming Mailbox 3	=	Outgoing Mailbox 3
Incoming Mailbox 4	=	Outgoing Mailbox 4
PCI Mailbox Empty/Full	=	Add-On Mailbox Empty/Full

A write to an outgoing mailbox also writes data into the incoming mailbox on the other interface. It also sets the status bits for the outgoing mailbox and the status bits for the incoming mailbox on the other interface. Reading the incoming mailbox clears all corresponding status bits in the Add-On and PCI mailbox status registers (AMBEF and MBEF).

For example, a PCI write is performed to the PCI outgoing mailbox 2, writing bytes 0 and 1 (BE0# and BE1# asserted). Reading the PCI Mailbox Empty/Full Status Register (MBEF) indicates that bits 4 and 5 are set. These bits indicate that outgoing mailbox 2, bytes 0 and 1 are full. Reading the Add-On Mailbox Empty/Full Status Register (AMBEF) shows that bits 4 and 5 in this register are also set, indicating Add-On incoming mailbox 2, bytes 0 and 1 are full. An Add-On read of incoming mailbox 2, bytes 0 and 1 clears the status bits in both the MBEF and AMBEF status registers.

To reset individual flags in the MBEF and AMBEF registers, the corresponding byte must be read from the incoming mailbox. The PCI and Add-On mailbox status registers, MBEF and AMBEF, are read-only. Mailbox flags may be globally reset from either the PCI interface or the Add-On interface. The PCI Bus Master Control/Status Register (MCSR) and the Add-On General Control/Status Register (AGCSTS) each have a bit to reset all of the mailbox status flags.

10.1.2 Mailbox Interrupts

The designer has the option to generate interrupts to the PCI and Add-On interfaces when specific mailbox events occur. The PCI and Add-On interfaces can each define two conditions where interrupts may be generated. An interrupt can be generated when an incoming mailbox becomes full and/or when an outgoing mailbox becomes empty. A specific byte within a specific mailbox is selected to generate the interrupt. The conditions defined to generate interrupts to the PCI interface do not have to be the same as the conditions defined for the Add-On interface. Interrupts are cleared through software as described in Section 10.3.2.

For incoming mailbox interrupts, when the specified byte becomes full, an interrupt is generated. The interrupt might be used to indicate command or status information has been provided, and must be read. For PCI incoming mailbox interrupts, the S5933 asserts the PCI interrupt, INTA#. For Add-On incoming mailbox interrupts, the S5933 asserts the Add-On interrupt, IRQ#.

For outgoing mailbox interrupts, when the specified byte becomes empty, an interrupt is generated. The interrupt might be used to indicate that the other interface has received the last information sent and more may be written. For PCI outgoing mailbox interrupts, the S5933 asserts the PCI interrupt, INTA#. For Add-On outgoing mailbox interrupts, the S5933 asserts the Add-On interrupt, IRQ#.

10.1.3 Add-On Outgoing Mailbox 4, Byte 3 Access

PCI incoming mailbox 4, byte 3 (Add-On outgoing mailbox 4, byte 3) does not function exactly like the other mailbox bytes. When an a serial nv memory boot device or no external boot device is used, the S5933 pins EA7:0 are redefined to provide direct external access to Add-On outgoing mailbox 4, byte 3. EA8 is redefined to provide a load clock which may be used to generate a PCI interrupt. The pins are redefined as follows:

Signal Pin	Add-On Outgoing Mailbox
EA0/EMB0	Mailbox 4, bit 24
EA1/EMB1	Mailbox 4, bit 25
EA2/EMB2	Mailbox 4, bit 26
EA3/EMB3	Mailbox 4, bit 27
EA4/EMB4	Mailbox 4, bit 28
EA5/EMB5	Mailbox 4, bit 29
EA6/EMB6	Mailbox 4, bit 30
EA7/EMB7	Mailbox 4, bit 31
EA8/EMBCLK	Mailbox 4, byte 3 load clock

If the S5933 is programmed to generate a PCI interrupt (INTA#), on an Add-On write to outgoing mailbox 4, byte 3, a rising edge on EMBCLK generates a PCI interrupt. The bits EMB7:0 can be read by the PCI bus interface by reading the PCI incoming mailbox 4, byte 3. These bits are useful to indicate various conditions which may have caused the interrupt.

When using the S5933 with a byte-wide boot device, the capability to generate PCI interrupts with Add-On hardware does not exist. In this configuration, PCI incoming mailbox 4, byte 3 (Add-On incoming mailbox 4, byte 3) cannot be used to transfer data from the Add-On - it always returns zeros when read from the PCI bus. This mailbox byte is sacrificed to allow the added functionality provided when a byte-wide boot device is not used.

10.2 BUS INTERFACE

The mailboxes appear on the Add-On and PCI bus interfaces as eight operation registers. Four are outgoing mailboxes, four are incoming mailboxes. The mailboxes may be used to generate interrupts to each of the interfaces. The following sections describe the Add-On and PCI bus interfaces for the mailbox registers.

10.2.1 PCI Bus Interface

The mailboxes are only accessible with the S5933 as a PCI target. The mailbox operation registers do not support burst accesses by an initiator. A PCI initiator attempting to burst to the mailbox registers causes the S5933 to respond with a target disconnect with data (Section 8.1.5.1.). PCI writes to full outgoing mailboxes overwrite data currently in that the mailbox. PCI reads from empty incoming mailboxes return the data that was previously contained in the mailbox. Neither of these situations cause a target retry or abort.

PCI incoming and outgoing mailbox interrupts are enabled in the Interrupt Control/Status Register (INTCSR). The mailboxes can generate a PCI interrupt (INTA#) under two conditions (individually enabled). For an incoming mailbox full interrupt, INTA# is asserted on the PCI clock rising edge after the Add-On mailbox write completes. For an outgoing mailbox empty interrupt, INTA# is asserted on the PCI clock rising edge after the Add-On mailbox read completes (the rising edge of RD#). INTA# is deasserted on the next PCI clock rising edge after the PCI access to clear the mailbox interrupt completes (TRDY# deasserted).

10.2.2 Add-On Bus Interface

The Add-On mailbox interface behaves similar to the PCI bus interface. Add-On writes to full outgoing mailboxes overwrite data currently in that mailbox. PCI reads from empty incoming mailboxes return the data that was previously contained in the mailbox.

Add-On incoming and outgoing mailbox interrupts are enabled in the Add-On Interrupt Control/Status Register (AINT). The mailboxes can generate the Add-On IRQ# interrupt under two conditions (individually enabled). For an incoming mailbox full interrupt, IRQ# is asserted one PCI clock period after the PCI mailbox write completes (TRDY# deasserted). For an outgoing mailbox empty interrupt, IRQ# is asserted one PCI clock period after the PCI mailbox read completes (TRDY# deasserted). IRQ# is deasserted immediately when the Add-On clears the mailbox interrupt (see Chapter 13 for exact timing).

When the S5933 is used with a serial nv memory boot device or no external boot device, the device pins EA8:0 are redefined as shown in Section 10.1.3. EA7:0 become EMB7:0 data inputs and EA8 becomes EMBCLK, a load clock. This configuration allows the Add-On to generate PCI interrupts with a low-to-high transition on EMBCLK. The PCI incoming mailbox interrupt must be enabled and set for mailbox 4, byte3 in the PCI Interrupt Control/Status Register (INTCSR). EMBCLK should begin high and be pulsed low, then high to be recognized (see Chapter 13 for exact timing). The rising edge of EMBCLK generates the interrupt. The rising edge of EMBCLK also latches in the values on EMB7:0. The S5933 interrupt logic must be cleared (INTA# deasserted) through INTCSR before further EMBCLK interrupts are recognized.

10.2.2.1 8-Bit and 16-Bit Add-On Interfaces

Some Add-On designs may implement an 8-bit or 16-bit bus interface. The mailboxes do not require a 32-bit Add-On interface. For 8-bit interfaces, the 8-bit data bus may be externally connected to all four bytes of the 32-bit Add-On interface (DQ 31:24, 23:16, 15:8, 7:0 are all connected). The Add-On device reading or writing the mailbox registers may access all mailbox bytes by cycling through the Add-On byte enable inputs. A similar solution applies to 16-bit Add-On buses. This solution works for Add-Ons which always use just 8-bit or just 16-bit accesses.

If the MODE pin is high, indicating a 16-bit Add-On interface, the previous solution may be modified for an 8-bit interface. The difference is that ADR1 must be toggled after the first two accesses to steer the S5933 internal data bus to the upper 16-bits of the mailboxes.

10.3 CONFIGURATION

The PCI interface and the Add-On interface each have four incoming mailboxes (IMBx or AIBMx) and four outgoing mailboxes (OMBx or AOMBx) along with a single mailbox status register (MBEF or AMBEF). Outgoing mailboxes are read/write, incoming mailboxes and the mailbox status registers are read-only.

The following sections discuss the registers associated with the mailboxes and accesses required for different modes of mailbox operation.

10.3.1 Mailbox Status

Every byte in each mailbox has a status bit in the Mailbox Empty/Full Status Registers (MBEF and AMBEF). Writing a particular byte into an outgoing mailbox sets the corresponding status bit in both the MBEF and AMBEF registers. A read of a 'full' byte in a mailbox clears the status bit. The MBEF and AMBEF are read-only. Status bits cannot cleared by writes to the status registers.

The S5933 allows the mailbox status bits to be reset through software. The Bus Master Control/Status (MCSR) PCI Operation Register and the Add-On General Control/Status (AGCSTS) Add-On Operation Register each have a bit to reset mailbox status. Writing a '1' to Mailbox Flag Reset bit in the MCSR or the AGCSTS register immediately clears all bits in the both the MBEF and AMBEF registers. Writing a '0' has no effect. The Mailbox Flag Reset bit is write-only.

The flag bits should be monitored when transferring data through the mailboxes. Checking the mailbox status before performing an operation prevents data from being lost or corrupted. The following sequences are suggested for PCI mailbox operations using status polling (interrupts disabled):

Reading a PCI Incoming Mailbox:

1) Check Mailbox Status. Read the mailbox status register to determine if any information has been passed from the Add-On interface.

MBEF	Bits 31:16	If a bit is set, valid data is contained in the corresponding mailbox byte.

2) Read Mailbox(es). Read the mailbox bytes which MBEF indicates are full. This automatically resets the status bits in the MBEF and AMBEF registers.

IMBx	Bits 31:0	Mailbox data.

Writing a PCI Outgoing Mailbox:

1) Check Mailbox Status. Read the mailbox status register to determine if information previously written to the mailbox has been read by the Add-On interface. Writes to full mailbox bytes overwrite data currently in the mailbox (if not already read by the Add-On interface). Repeat until the byte(s) to be written are empty.

MBEF	Bits 15:0	If a bit is set, valid data is contained in the corresponding mailbox byte and has not been read by the Add-On.

2) Write Mailbox(es). Write to the outgoing mailbox byte(s).

OMBx	Bits 31:0	Mailbox data.

Mailbox operations for the Add-On interface are functionally identical. The following sequences are suggested for Add-On mailbox operations using status polling (interrupts disabled):

Reading an Add-On Incoming Mailbox:

1) Check Mailbox Status. Read the mailbox status register to determine if any information has been passed from the PCI interface.

AMBEF	Bits 15:0	If a bit is set, valid data is contained in the corresponding mailbox byte.

2) Read Mailbox(es). Read the mailbox bytes which AMBEF indicates are full. This automatically resets the status bits in the AMBEF and MBEF registers.

AIMBx	Bits 31:0	Mailbox data.

Writing an Add-On Outgoing Mailbox:

1) Check Mailbox Status. Read the mailbox status register to determine if information previously written to the mailbox has been read by the PCI interface. Writes to full mailbox bytes overwrite data currently in the mailbox (if not already read by the PCI interface). Repeat until the byte(s) to be written are empty.

AMBEF	Bits 31:16	If a bit is set, valid data is contained in the corresponding mailbox byte and has not been read by the PCI bus.

2) Write Mailbox(es). Write to the outgoing mailbox byte(s).

AOMBx	Bits 31:0	Mailbox data.

10.3.2 Mailbox Interrupts

Although polling status is useful, in some cases, polling requires continuous actions by the processor reading or writing the mailbox. Mailbox interrupt capabilities are provided to avoid much of the processor overhead required by continuously polling status bits.

The Add-On and PCI interface can each generate interrupts on an incoming mailbox condition and/or an outgoing mailbox condition. These can be individually enabled/disabled. A specific byte in one incoming mailbox and one outgoing mailbox is identified to generate the interrupt(s). The tasks required to setup mailbox interrupts are shown below:

Enabling PCI mailbox interrupts:

1) Enable PCI outgoing mailbox interrupts. A specific byte within one of the outgoing mailboxes is identified to assert INTA# when read by the Add-On interface.

INTCSR	Bit 4	Enable outgoing mailbox interrupts
INTCSR	Bits 3:2	Identify mailbox to generate interrupt
INTCSR	Bits 1:0	Identify mailbox byte to generate interrupt

2) Enable PCI incoming mailbox interrupts. A specific byte within one of the incoming mailboxes is identified to assert INTA# when written by the Add-On interface.

INTCSR	Bit 12	Enable incoming mailbox interrupts
INTCSR	Bits 11:10	Identify mailbox to generate interrupt
INTCSR	Bits 9:8	Identify mailbox byte to generate interrupt

Enabling Add-On mailbox interrupts:

1) Enable Add-On outgoing mailbox interrupts. A specific byte within one of the outgoing mailboxes is identified to assert IRQ# when read by the PCI interface.

AINT	Bit 12	Enable outgoing mailbox interrupts
AINT	Bits 11:10	Identify mailbox to generate interrupt
AINT	Bits 9:8	Identify mailbox byte to generate interrupt

2) Enable Add-On incoming mailbox interrupts. A specific byte within one of the incoming mailboxes is identified to assert IRQ# when written by the PCI interface.

AINT	Bit 4	Enable incoming mailbox interrupts
AINT	Bits 3:2	Identify mailbox to generate interrupt
AINT	Bits 1:0	Identify mailbox byte to generate interrupt

With either the Add-On or PCI interface, these two steps can be performed with a single access to the appropriate register. They are shown separately here for clarity.

Once interrupts are enabled, the interrupt service routine must access the mailboxes and clear the interrupt source. A particular application may not require all of the steps shown. For instance, a design may only use incoming mailbox interrupts and not require support for outgoing mailbox interrupts. The interrupt service routine tasks are shown below:

Servicing a PCI mailbox interrupt (INTA#):

1) Identify the interrupt source(s). Multiple interrupt sources are available on the S5933. The interrupt service routine must verify that a mailbox generated the interrupt (and not some other interrupt source).

INTCSR	Bit 16	PCI outgoing mailbox interrupt indicator
INTCSR	Bit 17	PCI incoming mailbox interrupt indicator

2) Check mailbox status. The mailbox status bits indicate which mailbox bytes must be read or written.

MBEF	Bits 31:16	Full PCI incoming mailbox bytes
MBEF	Bits 15:0	Empty PCI outgoing mailbox bytes

3) Access the mailbox. Based on the contents of MBEF, mailboxes are read or written. Reading an incoming mailbox byte clears the corresponding status bit in MBEF.

OMBx	Bits 31:0	PCI outgoing mailboxes
IMBx	Bits 31:0	PCI incoming mailboxes

4) Clear the interrupt source. The PCI INTA# signal is deasserted by clearing the interrupt request. The request is cleared by writing a '1' to the appropriate bit.

INTCSR	Bit 16	Clear PCI outgoing mailbox interrupt
INTCSR	Bit 17	Clear PCI incoming mailbox interrupt

Servicing an Add-On mailbox interrupt (IRQ#):

1) Identify the interrupt source(s). Multiple interrupt sources are available on the S5933. The interrupt service routine must verify that a mailbox generated the interrupt (and not some other interrupt source).

AINT	Bit 16	Add-On incoming mailbox interrupt indicator
AINT	Bit 17	Add-On outgoing mailbox interrupt indicator

2) Check mailbox status. The mailbox status bits indicate which mailbox bytes must be read or written.

AMBEF	Bits 31:16	Empty Add-On outgoing mailbox bytes
AMBEF	Bits 15:0	Full Add-On incoming mailbox bytes

3) Access the mailbox. Based on the contents of AMBEF, mailboxes are read or written. Reading an incoming mailbox byte clears the corresponding status bit in AMBEF.

AIMBx	Bits 31:0	Add-On incoming mailboxes
AOMBx	Bits 31:0	Add-On outgoing mailboxes

4) Clear the interrupt source. The Add-On IRQ# signal is deasserted by clearing the interrupt request. The request is cleared by writing a '1' to the appropriate bit.

AINT	Bit 16	Clear Add-On incoming mailbox interrupt
AINT	Bit 17	Clear Add-On outgoing mailbox interrupt

In both cases, step 3 involves accessing the mailbox. To allow the incoming mailbox interrupt logic to be cleared, the mailbox status bit must also be cleared. Reading an incoming mailbox clears the status bits. Another option for clearing the status bits is to use the Mailbox Flag Reset bit in the MCSR and AGCSTS registers, but this clears all status bits, not just for a single mailbox or mailbox byte. For outgoing mailbox interrupts, the read of a mailbox register is what generated the interrupt; this ensures the status bits are already clear.