MicroLAB Systems

Ultimate DSP Development Solutions

DIGITAL SIGNAL PROCESSING

TORNADO-P64xx F/W rev.1A-1, rev.1A-2 and rev.1B

Ultra-High Performance 32-bit Fixed/Floating-Point TMS320C6x DSP Systems
for Host PCI-bus Computers and Stand-alone Applications

Addendum #2 to TORNADO-P6x User's Guide rev.4A

covers:
TORNADO-P6414/P6415/P6416 f/w rev.1A-1, rev.1A-2, rev.1B

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About this Document

This document contains addendum #2 to *TORNADO-P6x* User's Guide rev.4A and describes the firmware updates rev.1A-1 and rev.1A-2 for *TORNADO-P6414/P6415/P6416* rev.1A boards and the firmware rev.1B for *TORNADO-P6414/P6415/P6416* rev.1B boards.

This document replaces the earlier released addendum #1 to *TORNADO-P6x* User's Guide rev.4A, which described the firmware updates rev.1A-1 and rev.1A-2 for *TORNADO-P6414/P6415/P6416* rev.1A boards.

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Chapter 1. Introduction

This chapter contains general description for most recent updates to *TORNADO-P6x* DSP boards for PCI-bus, which have been introduced after release of *TORNADO-P6x* User's Guide rev.4A and which are not covered by that document.

1.1 Revision History

The following is the list of *TORNADO-P6x/P64xx* DSP boards for the PCI-bus, which have been introduced after release of *TORNADO-P6x* User's Guide rev.4A and which are covered by this addendum document:

- *TORNADO-P64xx* (*TORNADO-P6414/P6415/P6416*) rev.1A boards with firmware rev.1A-1 and rev.1A-2
- *TORNADO-P64xx* (*TORNADO-P6414/P6415/P6416*) rev.1B boards with all firmware revisions (so far firmware rev.1B only).

NOTE

There have been no updates introduced for *TORNADO-P62/P67/P6202/P6203* boards since release of *TORNADO-P6x* User's Guide rev.4A.

How to recognize firmware revision for your TORNADO-P64xx board and to check whether your TORNADO-P64xx board is covered by this addendum document

Follow the guidelines below in order to recognize whether your *TORNADO-P64xx* board is covered by this addendum document:

- download and install the latest *TORNADO Software Development Kit* (*TSDK*) from MicroLAB Systems FTP site (ftp://ftp.mlabsys.com/sft/tsdk/)
- run *TCC.EXE* command line *TSDK* utility from the Windows DOS prompt with the '-ih' command line option:

  TCC - ih
- observe the *TCC.EXE* output at DOS prompt window and locate the revision message. Valid revision messages are 'Rev.1A', 'Rev.1A-1', 'Rev.1A-2' and 'Rev.1B'.

Another way to recognize whether your *TORNADO-P64xx* board is covered by this addendum document *TORNADO-P64xx* board revision is to perform visual inspection of *TORNADO-P64xx* board and to locate the board hardware and firmware revision labeling information provided at the board :

- *TORNADO-P64xx* rev.1A boards with firmware rev.1A-1 and rev.1A-2 are visually recognized by means of the firmware revision label at the bottom of the board with the corresponding either 'f/w rev.1A-1' or 'f/w rev.1A-1' text on it. Instead, *TORNADO-P64xx* rev.1A boards with initial firmware rev.1A do not have such a label, and the board design revision (rev.1A) corresponds to the initial firmware revision.
- *TORNADO-P64xx* rev.1B boards have a different board design versus *TORNADO-P64xx* rev.1A boards and all have the firmware labeling information at the bottom of the board.

Finally, user DSP application can recognize the firmware rev.1A-1, rev.1A-2 and rev.1B by means of reading the firmware revision ID bit-field of *DSP_DEV_ID_RG* I/O control register from the DSP environment as it described later in this document. Host PC application can recognize the firmware rev.1A-1, rev.1A-2 and rev.1B by reading the firmware revision ID byte of the PCIC nvRAM memory as it described later in this document

1.2 Software Compatibility Issues

User DSP and host PC application software, which has been designed for initial firmware rev.1A of *TORNADO-P64xx* boards, which are covered by *TORNADO-P6x* User's Guide, generally do not need any modifications in order to run at *TORNADO-P64xx* boards with the firmware rev.1A-1, rev.1A-2 and rev.1B. The only requirements which may apply is to recompile already designed either DSP or host PC application with latest release of the corresponding *TORNADO-P6x* software utilities as it is described below.

DSP software compatibility

User DSP application software, which has been designed for initial firmware rev.1A of *TORNADO-P64xx* boards, which are covered by *TORNADO-P6x* User's Guide, do not need any modifications in order to run at *TORNADO-P64xx* boards with the firmware rev.1A-1, rev.1A-2 and rev.1B. The only requirement which applies is to recompile already designed user DSP applications with the latest release of *TORNADO-P6x* DSP software utilities (*TP6X_DSP.H* file).

NOTE

TORNADO-P6x DSP software utilities (*TP6X_DSP.H* file) come standard with all *TORNADO-P6x* boards and are available for free download from MicroLAB Systems FTP site (ftp://ftp.mlabsys.com).

However, in case user DSP application for initial firmware rev.1A of *TORNADO-P64xx* boards has been designed without DSP software utilities for *TORNADO-P6x* boards, which come standard with these boards, then the minor modifications are required in order to comply with firmware rev.1A-1, rev.1A-2 and rev.1B of *TORNADO-P64xx* boards and apply to the initialization procedure for the TMS320C64xx DSP on-chip EMIF control registers as it is described later in this document.

NOTE

In order to stay up-to-date with the latest firmware modification and to minimize the software design efforts, it is recommended that user DSP applications for *TORNADO-P6x* boards are being designed using the latest release of *TORNADO-P6x* DSP software utilities, which come standard with all *TORNADO-P6x* boards and which are available from MicroLAB Systems FTP-site (ftp://ftp.mlabsys.com).

Extra DSP software modifications, which may be required, apply to the DSP timing issues (DSP on-chip timers programming, software loop delays, etc) in case the on-board TMS320C64xx DSP chip installed feature increased DSP clock frequency (either 600 MHz, or 720 MHz, or 1 GHz) and to the on-board FLASH access and programming procedures for *TORNADO-P64xx* rev.1B boards, which provide embedded high-capacity FLASH memory.

There are no backward software compatibility issues known for running user DSP applications, which have been designed for *TORNADO-P64xx* boards with firmware rev.1A-1, rev.1A-2 and rev.1B, at *TORNADO-P64xx* boards with initial firmware rev.1A in case user DSP application has been designed using the latest release of *TORNADO-P6x* DSP software utilities and in case the DSP application does not utilize the on-board hardware resources, which are not available for *TORNADO-P64xx* rev.1A boards. However, this requires clear understanding of all hardware update details for different firmware revision, which are described below in this document.

Host PC software compatibility

User host PC application software, which has been designed for initial firmware rev.1A of *TORNADO-P64xx* boards, does not require any modification in order to run at *TORNADO-P64xx* boards with firmware rev.1A-1, rev.1A-2 and rev.1B in case either *TORNADO-P6x* host PC DOS utilities or *TORNADO Software Development Kit* (*TSDK*) for Windows are used to design user host PC application.

NOTE

Both *TORNADO-P6x* host PC DOS utilities and *TSDK* for Windows come standard with all *TORNADO-P6x* boards and are available for free download from MicroLAB Systems FTP site (ftp://ftp.mlabsys.com).

However, in case user host PC application has been designed without either *TORNADO-P6x* host PC DOS utilities or *TSDK*, then the only possible modification required refers to the setting of DSP on-chip EMIF control registers in case user application performs access to the DSP environment via DSP on-chip HPI port prior starting DSP application (HPI bootmode).

NOTE

In order to stay up-to-date with the latest firmware modification and to minimize the software design efforts, it is recommended that user host PC applications for *TORNADO-P6x* boards are being designed using the latest release of either *TORNADO-P6x* host PC DOS utilities or *TSDK* software, which come standard with all *TORNADO-P6x* boards and which are available from MicroLAB Systems FTP-site (ftp://ftp.mlabsys.com).

Chapter 2. System Architecture and Construction

This chapter contains detail description for the new features available in the new firmware revisions of *TORNADO-P64xx* boards.

2.1 New features available in *TORNADO-P64xx* boards with firmware rev.1A-1, rev.1A-2 and rev.1B

The following is a detail list of hardware updates for *TORNADO-P64xx* boards with firmware rev.1A-1, rev.1A-2 and rev.1B versus rev.1A:

- The TMS320C64xx DSP memory map has been updated to include new *DSP_XMEM_LEN_ID_RG* DSP IOX register (firmware rev.1A-1, rev.1A-2 and rev.1B), *DSP_XMEM2_LEN_ID_RG* DSP IOX register (firmware rev.1B), and *DSP_FLASH_PAGE_RG* DSP IOX register (firmware rev.1B). Refer to section 2.2 later in this chapter for more details about updated DSP memory map.
- The DSP EMIF-A clock does not depend upon the DSP clock and is equal to 125 MHz for firmware rev.1A-1 and to 133 MHz for firmware rev.1A-2 and rev.1B. This allows to increase the SBSRAM/SDRAM/DPRAM data transfer performance by 25% and 33% correspondingly if compared to *TORNADO-P64xx* boards with 600 MHz DSP and initial firmware rev.1A. This modification requires the corresponding EMIF control register settings updates as it is described in section 2.3 later in this chapter.
- The firmware revision ID field of the *DSP_DEV_REV_ID_RG* read-only DSP IOX register from the DSP environment reads as 2H, 3H and 4H for firmware rev.1A-1, rev.1A-2 and rev.1B correspondingly in order the DSP application could recognize the firmware revision and to perform applicable DSP environment configuration actions as required. Refer to section 2.4 later in this chapter for more details.
- A format of *DSP_XIO_FMT_RG* DSP IOX register has been modified to include new DSP clock ID bit field for firmware rev.1A-1, rev.1A-2 and rev.1B, which returns the ID code for the DSP clock frequency (600 MHz, 720 MHz and 1 GHz). Given that, a user DSP application can correctly handle all applicable timing issues (programming of the DSP on-chip timers, software loop delays, etc) and will therefore appear compatible with all speed grades of on-board TMS320C64xx DSP. Refer to section 2.5 later in this chapter for more details.
- New *DSP_XMEM_LEN_ID_RG* read-only DSP IOX register (firmware rev.1A-1, rev.1A-2 and rev.1B) returns the ID codes for on-board SBSRAM, SDRAM and DPRAM capacities. Given that, a user DSP application can detect the on-board SBSRAM/SDRAM/DPRAM capacity in order to correspondingly configure the DSP on-chip EMIF-A SDRAM control registers and application environment variables for external memory pools, etc. Refer to section 2.6 later in this chapter for more details.
- The firmware revision ID location (address 23H) of on-board PCIC nvRAM memory has been modified to return the 02H, 03H and 04H values for firmware rev.1A-1, rev.1A-2 and rev.1B correspondingly in order host PC application could recognize the firmware revision and to perform applicable actions as required. Refer to section 2.7 later in this chapter for more details.
- New hardware rev.1B of *TORNADO-P64xx* board (firmware rev.1B) features a different board design versus the hardware rev.1A of *TORNADO-P64xx* boards (firmware revisions rev.1A,

rev.1A-1 and rev.1A-2). Refer to section 2.8 for more details about design of *TORNADO-P64xxQ* rev.1B board. The following is a list of new hardware features available in *TORNADO-P64xxQ* rev.1B board versus rev.1A board:

- ☐ *TORNADO-PX64xxQ* rev.1B board provides the embedded (soldered-in) high-density FLASH memory with 512K..64Mx8 capacity instead of the on-board FLASH/EPROM PLCC-32 socket (S1) for plug-in either 512Kx8 FLASH or 1Mx8 EPROM memory at on *TORNADO-PX64xx* rev.1A board. Refer to sections 2.8 and 2.9 for more details.
- ☐ *TORNADO-PX64xxQ* rev.1B provides a modified on-board SW3 switch, which is used for write protection control of on-board FLASH memory. Refer to sections 2.8 and 2.9 for more details.
- ☐ *TORNADO-PX64xxQ* rev.1B provides new *DSP_XMEM2_LEN_ID_RG* and *DSP_FLASH_PAGE_RG* DSP IOX registers, which are used for identification of the on-board FLASH memory capacity and for selection of a 1Mx8 FLASH memory page for current access (for FLASH capacity 2M and larger). Refer to section 2.9 for more details.
- ☐ *TORNADO-PX64xxQ* rev.1B provides the on-board SW5-4 switch, which is used for write protection control of on-board PCIC nvRAM. Refer to section 2.10 for more details.

The corresponding sections below provide details about all new features and/or the corresponding update information applicable to the new hardware and firmware revisions of *TORNADO-P64xx* boards.

2.2 Updated TMS320C64xx DSP memory map

In firmware rev.1A-1 and rev.A-2, the DSP memory map for *TORNADO-P64xx* DSP controllers have been updated to include new *DSP_XMEM_LEN_ID_RG* read-only external I/O control registers as it is shown below in the table [2-1b], which is an update for the table 2-1b from *TORNADO-P6x* User's Guide rev.4A.

Table [2-1b]. Memory map for TMS320C64xx DSP of *TORNADO-P64xx* DSP systems.

memory area of TMS320C64xx DSP	DSP address range (in bytes)	valid data bits	value at DSP RESET	Access mode	wait states	EMIF CE area and mode
On-board (DSP off-chip) memories						
SBSRAM	80000000H ..800FFFFFH (128Kx64) 80000000H ..801FFFFFH (256Kx64) 80000000H ..803FFFFFH (512Kx64)	D0..D31	-	r/w	0	EMIF-A CE-0 SBSRAM mode

DPRAM	90000000H ..9007FFFFH (128Kx32) 90000000H ..900FFFFFH (256Kx32) 90000000H ..901FFFFFH (512Kx32)	D0..D31	-	r/w	0	EMIF-A CE-1 SBSRAM mode
DPRAM: *DPRAM_HM_RQ* register (PCI-to-DSP interrupt request via DPRAM) (256K/512Kx32 DPRAM only)	000FFFFCH (256Kx32) 001FFFFCH (512Kx32)	D0..D31	-	r/w	0	
DPRAM: *DPRAM_MH_RQ* register (DSP-to-DSP interrupt request via DPRAM) (256K/512Kx32 DPRAM only)	000FFFF8H (256Kx32) 001FFFF8H (512Kx32)	D0..D31	-	r/w	0	
SDRAM	A0000000H ..A1FFFFFFH (4Mx64) A0000000H ..A7FFFFFFH (16Mx64)	D0..D31	-	r/w	0	EMIF-A CE-2 SDRAM mode
FLASH/EPROM	64000000H ..640FFFFFH (1Mx8)	D0..D7 @W8	-	r/w @A8 (with h/w write enable)	FWS	EMIF-B CE-1 8-bit ASYNC mode
AMCC S5933 PCIC and IOX registers						
S5933 PCIC area: *DSP_PCIC_FIFO_RG* register (32-bit data format only) (Read-FIFO and Write-FIFO)	60000000H	D0..D31 @W32	-	r/w @A32	AWS +[3)]	CE-0 ASYNC mode
S5933 PCIC area: *DSP_PCIC_AMBEF_RG* register	60000004H	D0..D31 @W32	-	R	AWS +[3)]	
S5933 PCIC area: *DSP_PCIC_AINT_RG* register	60000008H	D0..D31 @W32	-	r/w	AWS +[3)]	

S5933 PCIC area: *DSP_PCIC_AGCSTS_RG* register	6000000CH	D0..D31 @W32	-	r/w	AWS +[3)]
S5933 PCIC area: *DSP_PCIC_MWAR_RG* register	60000010H	D0..D31 @W32	-	r/w	AWS +[3)]
S5933 PCIC area: *DSP_PCIC_MWTC_RG* register	60000014H	D0..D31 @W32	-	r/w	AWS +[3)]
S5933 PCIC area: *DSP_PCIC_MRAR_RG* register	60000018H	D0..D31 @W32	-	r/w	AWS +[3)]
S5933 PCIC area: *DSP_PCIC_MRTC_RG* register	6000001CH	D0..D31 @W32	-	r/w	AWS +[3)]
S5933 PCIC area: *DSP_PCIC_IMBX0_RG* register (Incoming MBX-1)	60000020H	D0..D31 @W32	-	R	AWS +[3)]
S5933 PCIC area: *DSP_PCIC_IMBX1_RG* register (Incoming MBX-2)	60000024H	D0..D31 @W32	-	R	AWS +[3)]
S5933 PCIC area: *DSP_PCIC_IMBX2_RG* register (Incoming MBX-3)	60000028H	D0..D31 @W32	-	R	AWS +[3)]
S5933 PCIC area: *PCIC_IMBX3_RG* register (Incoming MBX-4)	6000002CH	D0..D31 @W32	-	R	AWS +[3)]
S5933 PCIC area: *DSP_PCIC_OMBX0_RG* register (Outgoing MBX-1)	60000030H	D0..D31 @W32	-	r/w	AWS +[3)]
S5933 PCIC area: *DSP_PCIC_OMBX1_RG* register (Outgoing MBX-2)	60000034H	D0..D31 @W32	-	r/w	AWS +[3)]
S5933 PCIC area: *DSP_PCIC_OMBX2_RG* register (Outgoing MBX-3)	60000038H	D0..D31 @W32	-	r/w	AWS +[3)]
S5933 PCIC area: *DSP_PCIC_OMBX3_RG* register (Outgoing MBX-4)	6000003CH	D0..D31 @W32	-	r/w	AWS +[3)]

IOX area: *DSP_FIFO_STAT_RG* register (PCIC FIFO status)	60000040H	D0..D7 @W32	-	R	AWS
IOX area: *DSP_AWREN_RG* register (PCI-bus mastering control)	60000044H	D0..D7 @W32	0	r/w	AWS
IOX area: *DSP_XMEM_LEN_ID_RG* register (SBSRAM/SDRAM/ DPRAM capacity ID for *TORNADO-P64xx* f/w rev.1A-1, rev.1A-2, rev.1B)	60000048H	D0..D7 @W32	-	r	AWS
IOX area: *DSP_XIO_FMT_RG* register (external I/O format control)	6000004CH	D0..D7 @W32	0	r/w	AWS
IOX area: *MH_RQ* register (DSP-to-PCI request)	60000050H	Write data is ignored @W32	-	W	AWS
IOX area: *DSP_PXSX_RESET_RG* register (reset control for PIOX and SIOX DCM sites)	60000054H	D0..D7 @W32	0	r/w	AWS
IOX area: *DSP_SYS_STAT_RG* register (system information)	60000058H	D0..D7 @W32	-	R	AWS
IOX area: *DSP_WDT_CLR_RG* register (clear watch-dog timer)	6000005CH	Write data is ignored @W32	-	W	100ns (hardware controlled) + AFWS
IOX area: *DSP_DEV_ID_RG* register (device ID)	6000005CH	D0..D7 @W32	-	R	AWS
IOX area: *DSP_WDT_EN_RG* register (WDT enable for stand-alone operation)	60000060H	D0..D7 @W32	0	r/w	AWS
IOX area: *DSP_HM_RQ0_RG* register (PCI-to-DSP request #0)	60000064H	D0..D7 @W32 write data is ignored	-	R w	AWS

IOX area: *DSP_HM_RQ1_RG* register (PCI-to-DSP request #1)	60000068H	D0..D7 @W32 write data is ignored	-	R w	AWS	
IOX area: *DSP_NMI_SEL_RG* register (DSP NMI source selector)	6000006CH	D0..D7 @W32	0H	r/w	AWS	
IOX area: *DSP_EXT_INT4_SEL_RG* register (DSP EXT_INT4 source selector)	60000070H	D0..D7 @W32	0H	r/w	AWS	
IOX area: *DSP_EXT_INT5_SEL_RG* register (DSP EXT_INT5 source selector)	60000074H	D0..D7 @W32	0H	r/w	AWS	
IOX area: *DSP_EXT_INT6_SEL_RG* register (DSP EXT_INT6 source selector)	60000078H	D0..D7 @W32	0H	r/w	AWS	
IOX area: *DSP_EXT_INT7_SEL_RG* register (DSP EXT_INT7source selector)	6000007CH	D0..D7 @W32	0H	r/w	AWS	
IOX area: *DSP_FLASH_PAGE_RG* register (FLASH page selector for *TORNADO-P64xx* firmware rev.1B)	60080000H	D0..D7 @W32	0	r/w	AWS	
IOX area: *DSP_XMEM2_LEN_ID_RG* register (FLASH capacity ID for *TORNADO-P64xx* f/w rev.1B)	60080004H	D0..D7 @W32	-	r	AWS	
Parallel data buses of on-board DCM sites						
Parallel data bus of SIOX-A rev.C DCM site interface	60100000H ..6010007FH	D0..D7 @W32	-	r/w	AWS +*SXA_RDY*	EMIF-B CE-0 ASYNC mode

Parallel data bus of SIOX-B rev.C DCM site interface	60180000H ..6018007FH	D0..D7 @W32	-	r/w	AWS +*SXB_RDY*	
Parallel data bus of PIOX DCM site interface	6C000000H ..6C1FFFFFH	D0..D31 @W32	-	r/w	AWS +*PX_RDY*	EMIF-B CE-3 ASYNC mode
Parallel data bus of PIOX-16 DCM site interface	6C000000H ..6C03FFFFH	D0..D15 @W32	-	r/w @A16 @A32	AWS +*PX_RDY*	
DSP on-chip memory and peripheral registers						
DSP on-chip RAM	00000000H ..000FFFFFH	D0..D31	-	r/w	-	-
DSP on-chip peripheral registers	01800000H ..02000033H	D0..D31	-	r/w	-	-

Notes:

1. DSP IOX area denotes DSP I/O expansion registers.
2. S5933 PCIC area denotes AMCC S5933 PCI Matchmaker Controller AOB operation registers.
3. Accesses to the AOB registers of S5933 PCI Matchmaker Controller require additional wait states depending upon the type of current host PCI-bus interface operation and eventual synchronization between the PCI-bus clock and the DSP clock.
4. *AWS* denotes number of software programmed wait states for accessing corresponding asynchronous EMIF-A/B CE area, which is a sum of read/write strobe wait states, read/write setup wait states and read/write hold wait states. Refer to the corresponding subsection below for more details.
5. *AFWS* denotes number of software programmed framing wait states for accessing asynchronous EMIF CE-0 area, which is a sum of read/write setup wait states and read/write hold wait states. Refer to the corresponding subsection below for more details.
6. *SXA_RDY*, *SXB_RDY* and *PX_RDY* denote extra wait states, which can be generated by external hardware ready signals for on-board SIOX-A rev.C site, SIOX-B rev.C site and PIOX/PIOX-16 DCM sites. Refer to the corresponding subsection below for more details about DPRAM and the corresponding sections later in this chapter for more details about SIOX and PIOX/PIOX-16 DCM sites.
7. @W16 and @W32 denote that the address step for consecutive data words of this area corresponds to 16-bit and 32-bit data words correspondingly. Refer to the corresponding subsection below for more details.
8. Other DSP memory and I/O areas are reserved. Do not use these address areas.
9. Register access modes: *r* - read only, *w* - write only, *r/w* - read/write.
10. If specified in the ‘access mode’ field, the ‘@A8’ denotes that access can be performed using 8-bit word only, the ‘@A16’ denotes that access can be performed using 16-bit word only, and ‘@A32’ denotes that access can be performed using 32-bit word only. If none of the above is specified in the ‘access mode’ field, then access can be performed using any of 8/16/32-bit words.
11. Highlighted DSP IOX registers are available for *TORNADO-P64xx* boards with firmware rev.1A-1, rev.1A-2 and rev.1B, and are not described in *TORNADO-P6x* User’s Guide rev.4A.

2.3 Updated settings for the TMS320C64xx DSP on-chip EMIF control registers

The TMS320C64xx DSP on-chip EMIF-A/B control registers are set upon the *TORNADO-P64xx* board firmware revision as it is listed below in table [2-3b], which is an update for the table 2-3b from *TORNADO-P6x* User's Guide rev.4A.

Table [2-3b]. Recommended EMIF registers settings for TMS320C64xx DSP of *TORNADO-P64xx* DSP systems.

TMS320C64xx DSP on-chip EMIF control register	**EMIF area mode**	***TORNADO-P64xx f/w rev.1A*** (600 MHz DSP clock, 100MHz EMIF-A/B clock)	***TORNADO-P64xx f/w rev.1A-1*** (600/720/1000 MHz DSP clock, 125MHz EMIF-A/B clock)	***TORNADO-P64xx f/w rev.1A-2 and rev.1B*** (600/720/1000 MHz DSP clock, 133MHz EMIF-A/B clock)
EMIF-A interface control registers				
EMIF-A Global Control Register (EMIFA_GBLCTL)	-	0x0001207c	0x0001207c	0x0001207c
EMIF-A CE-0 Space Control Register (EMIFA_CE0CTL) *(area controls 64-bit SBSRAM)*	64-bit SBSRAM	0x000000e0	0x000000e0	0x000000e0
EMIF-A CE-0 Space Secondary Control Register (EMIFA_CE0SEC)		0x00000002	0x00000002	0x00000002
EMIF-A CE-1 Space Control Register (EMIFA_CE1CTL) *(area controls 32-bit synchronous DPRAM)*	32-bit SBSRAM	0x00000040	0x00000040	0x00000040
EMIF-A CE-1 Space Secondary Control Register (EMIFA_CE1SEC)		0x00000002	0x00000002	0x00000002
EMIF-A CE-2 Space Control Register (EMIFA_CE2CTL) *(area controls 64-bit SDRAM)*	64-bit SDRAM	0x000000d0	0x000000d0	0x000000d0
EMIF-A CE-2 Space Secondary Control Register (EMIFA_CE2SEC)		0x00000002	0x00000002	0x00000002

EMIF-A CE-3 Space Control Register (EMIFA_CE3CTL) *(area is reserved)*	8-bit ASYNC (reserved)	0xffffff03	0xffffff03	0xffffff03
EMIF-A CE-3 Space Secondary Control Register (EMIFA_CE3SEC)		x	x	x
EMIF-A SDRAM Control Register (EMIFA_SDCTL)	-	0x57115000 (SDRAM 4Mx64) 0x63115000 (SDRAM 16Mx64)	0x57117000 (SDRAM 4Mx64) 0x63117000 (SDRAM 16Mx64)	0x57115000 (SDRAM 4Mx64) 0x63117000 (SDRAM 16Mx64)
EMIFA SDRAM Extension Register (EMIFA_SDEXT)	-	0x00014d29	0x00014d29	0x00014d29
EMIFA SDRAM Timing Register (EMIFA_SDTIM)	-	1562 (SDRAM 4Mx64) 781 (SDRAM 16Mx64)	1952 (SDRAM 4Mx64) 976 (SDRAM 16Mx64)	2082 (SDRAM 4Mx64) 1041 (SDRAM 16Mx64)
EMIF-B interface control registers				
EMIF-B Global Control Register (EMIFB_GBLCTL)	-	0x0001207c	0x0001207c	0x0001207c
EMIF-B CE-0 Space Control Register (EMIFB_CE0CTL) *(area controls PCIC, IOX, SIOX-A/B rev.C sites)*	16-bit ASYNC	0x10d14311 strobe: 3 clk (30ns) setup: 1 clk (10ns) hold: 1 clk (10ns)	0x21124411 strobe: 4 clk (32ns) setup: 2 clk (16ns) hold: 1 clk (8ns)	0x21124411 strobe: 4 clk (30ns) setup: 2 clk (15ns) hold: 1 clk (7.5ns)
EMIF-B CE-0 Space Secondary Control Register (EMIFB_CE0SEC)		x	x	x
EMIF-B CE-1 Space Control Register (EMIFB_CE1CTL) *(area controls 8-bit FLASH/EPROM)*	8-bit ASYNC (ROM)	0x22924a01 strobe: 10 clk (100ns) setup: 2 clk (20ns) hold: 1 clk (10ns)	0x23524d01 strobe:13 clk (104ns) setup: 2 clk (16ns) hold: 1 clk (8ns)	***f/w rev.1A-2:*** 0x23d24e01 strobe:14 clk (100ns) setup: 2 clk (15ns) hold: 1 clk (7.5ns) ***f/w rev.1B:*** 0x24125001 strobe:16 clk (120ns) setup: 2 clk (15ns) hold: 1 clk (7.5ns)

EMIF-B CE-1 Space Secondary Control Register (EMIFB_CE1SEC)		x	x	x
EMIF-B CE-2 Space Control Register (EMIFB_CE2CTL) *(area is reserved)*	8-bit ASYNC (reserved)	0xffffff03	0xffffff03	0xffffff03
EMIF-B CE-2 Space Secondary Control Register (EMIFB_CE2SEC)		x	x	x
EMIF-B CE-3 Space Control Register (EMIFB_CE3CTL) *(area controls PIOX/PIOX-16 DCM site)*	16-bit ASYNC (reserved)	0x10d14311 r/w strobe: 3 clk (30ns) r/w setup: 1 clk (10ns) r/w hold: 1 clk (10ns)	0x21124411 strobe: 4 clk (32ns) setup: 2 clk (16ns) hold: 1 clk (8ns)	0x21124411 strobe: 4 clk (30ns) setup: 2 clk (15ns) hold: 1 clk (7.5ns)
EMIF-B CE-3 Space Secondary Control Register (EMIFB_CE3SEC)		x	x	x
EMIF-B SDRAM Control Register (EMIFB_SDCTL)	-	x	x	x
EMIFB SDRAM Extension Register (EMIFB_SDEXT)	-	x	x	x
EMIFB SDRAM Timing Register (EMIFB_SDTIM)	-	x	x	x

Notes: 1. *TORNADO-P64xx* EMIF-A/B clock is 100 MHz (10 ns clock cycle) for f/w rev.1A, is 125 MHz (8ns clock cycle) for f/w rev.1A-1 and is 133 MHz (7.5ns clock cycle) for f/w rev.1A-2 and rev.1B.
2. 'X' denotes don't care value.

2.4 Updated firmware revision ID bit-field of *DSP_DEV_ID_RG* IOX register

TORNADO-P64xx boards provide the *DSP_DEV_ID_RG* read-only IOX register from the DSP environment, which returns a 4-bit device ID code and 4-bit firmware revision ID code.

DSP_DEV_ID_RG IOX register (read-only)
(*TORNADO-P64xx* boards with all firmware revisions)

X	*REV_ID-3 (r)*	*REV_ID-2 (r)*	*REV_ID-1 (r)*	*REV_ID-0 (r)*	*DEV_ID-3 (r)*	*DEV_ID-2 (r)*	*DEV_ID-1 (r)*	*DEV_ID-0 (r)*
Bit-31...bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

The values of 4-bit firmware revision ID code, which is returned for different firmware revisions of *TORNADO-P64xx* boards, are shown in table 2-X1 below (this table is an add-on to *TORNADO-P64xx* User's Guide rev.4A).

Table 2-X1. Firmware revision ID codes available via the *DSP_DEV_ID_RG* I/O control register of *TORNADO-P64xx* boards.

register bit(s)	Access mode	Description
{*REV_ID-3..0*}	R	Returns a firmware revision ID code. {*REV_ID-3..0*} = {0,0,0,1} setting corresponds to initial firmware rev.1A of *TORNADO-P64xx* boards with 600MHz DSP (100MHz EMIF-A/B clock frequency). {*REV_ID-3..0*} = {0,0,1,0} setting corresponds to the firmware rev.1A-1 of *TORNADO-P64xx* rev.1A boards with 600/720/1000MHz DSP (125MHz EMIF-A/B clock frequency). {*REV_ID-3..0*} = {0,0,1,1} setting corresponds to the firmware rev.1A-2 of *TORNADO-P64xx* rev.1A boards with 600/720/1000MHz DSP (133MHz EMIF-A/B clock frequency). {*REV_ID-3..0*} = {0,1,0,0} setting corresponds to the firmware rev.1B of *TORNADO-P64xx* rev.1B boards with 600/720/1000MHz DSP (133MHz EMIF-A/B clock frequency). Other {*REV_ID-3..0*} codes are reserved for future expansion.

Notes: 1. The highlighted values correspond to the new settings available for *TORNADO-P64xx* boards with firmware rev.1A-1, rev.1A-2 and rev.1B.

2.5 DSP clock ID field in *DSP_XIO_FMT_RG* IOX register

TORNADO-P64xx boards with firmware rev.1A-1, rev.1A-2 and rev.1B provide new {*DSP_CLK_ID-1..0*} read-only bit-field for *DSP_XIO_FMT_RG* read-only DSP IOX register from the DSP environment, which returns a 2-bit DSP clock frequency ID code.

DSP_XIO_FMT_RG IOX register (r/w)
(*TORNADO-P64xx* boards with all firmware revisions)

X	*0*	*0*	*DSP_CLK_ID-1 (r)*	*DSP_CLK_ID-0 (r)*	*0*	*PCIC_FMT (r/w, 1+)*	*PX_FMT-1 (r/w, 0+)*	*PX_FMT-0 (r/w, 0+)*
bit-31...bit-8	Bit-7	bit-6	bit-5	Bit-4	bit-3	bit-2	bit-1	bit-0

The DSP clock frequency ID code is used to identify the DSP clock frequency and to correspondingly adjust the timing parameters of a user DSP application (programming of the DSP on-chip timers, software loop delays, programming the bit rate frequency of DSP on-chip McBSP ports, etc) and thus making an application compatible with all speed grades of TMS320C64xx DSP used in *TORNADO-P64xx* boards.

Table [2-8] below is an add-on to table 2-8 of *TORNADO-P6x* User's Guide rev.4A and provides a list of DSP clock frequency ID codes for all firmware revisions of *TORNADO-P64xx* boards.

Table [2-8]. DSP clock frequency ID codes available via the DSP clock ID bit-field of the *DSP_XIO_FMT_RG* DSP IOX register of *TORNADO-P64xx* boards.

register bit(s)	Access mode	Description
{*DSP_CLK_ID-1..0*}	R	Returns a DSP clock frequency ID code. {*DSP_CLK_ID-1..0*} = {0,0} setting corresponds to the 600MHz speed grade of TMS320C64xx DSP. Since this is the default value returned by bits #4..5 of the *DSP_XIO_FMT_RG* DSP IOX register of *TORNADO-P64xx* boards with f/w rev.1A, which have been manufactured with the 600 MHz speed grade only of TMS320C64xx DSP, then this setting can be considered available for all firmware revisions including the rev.1A. {*DSP_CLK_ID -1..0*} = {0,1} setting corresponds to the 720MHz speed grade of TMS320C64xx DSP. This setting is available for firmware rev.1A-1, rev.1A-2 and rev.1B only. {*DSP_CLK_ID -1..0*} = {1,0} setting corresponds to the 1GHz speed grade of TMS320C64xx DSP. This setting is available for firmware rev.1A-1, rev.1A-2 and rev.1B only. {*DSP_CLK_ID -1..0*} = {1,1} setting is reserved.

Notes: 1. The highlighted values correspond to the new settings available for *TORNADO-P64xx* boards with firmware rev.1A-1, rev.1A-2 and rev.1B.

2.6 *DSP_XMEM_LEN_ID_RG* IOX register

TORNADO-P64xx boards with firmware rev.1A-1, rev.1A-2 and rev.1B provide new *DSP_XMEM_LEN_ID_RG* read-only IOX register for the DSP environment, which returns the ID codes for on-board SBSRAM, SDRAM and DPRAM memory capacities.

DSP_XMEM_LEN_ID_RG I/O control register (r)
(*TORNADO-P64xx* boards with firmware rev.1A-1, rev.1A-2 and rev.1B only)

X	*0*	*0*	*DPRAM_ LEN_ID-1 (r)*	*DPRAM_ LEN_ID-0 (r)*	*SDRAM_ LEN_ID-1 (r)*	*SDRAM_ LEN_ID-0 (r)*	*SBSRAM_ LEN_ID-1 (r)*	*SBSRAM_ LEN_ID-0 (r)*
bit-31...bit-8	Bit-7	bit-6	bit-5	Bit-4	bit-3	bit-2	bit-1	bit-0

SBSRAM/SDRAM/DPRAM capacity ID codes are used to identify the on-board DSP external memory capacity in order to correspondingly configure the DSP on-chip EMIF-A SDRAM control registers and to correspondingly set the DSP application environment variables for external memory pools, etc. Furthermore, the DPRAM capacity ID code also allows to identify whether the DPRAM memory provides dedicated locations for generation of the Host-to-DSP and DSP-to-Host interrupt requests via DPRAM, which are available for 256Kx32 and 512Kx32 DPRAM memories only.

NOTE

The *DSP_XMEM_LEN_ID_RG* read-only DSP IOX register is not available in *TORNADO-P64xx* boards with initial firmware rev.1A.

Table 2-X2 below (this table is an add-on to *TORNADO-P64xx* User's Guide rev.4A) provides a list of SBSRAM/SDRAM/DPRAM capacity ID codes available for the firmware rev.1A-1 and rev.1A-2 of *TORNADO-P64xx* boards.

Table 2-X2. SBSRAM/SDRAM/DPRAM capacity ID codes available via the *DSP_XMEM_LEN_ID_RG* IOX register of *TORNADO-P64xx* boards with f/w rev.1A-1 and rev.1A-2.

register bit(s)	access mode	Description
{*SBSRAM_LEN_ID-1..0*}	R	Returns a capacity ID code for on-board SBSRAM memory bank. {*SBSRAM_LEN_ID-1..0*} = {0,0} setting corresponds to no SBSRAM memory installed. {*SBSRAM_LEN_ID-1..0*} = {0,1} setting corresponds to the 128Kx64 SBSRAM memory installed. {*SBSRAM_LEN_ID-1..0*} = {1,0} setting corresponds to the 256Kx64 SBSRAM memory installed. {*SBSRAM_LEN_ID-1..0*} = {1,1} setting corresponds to the 512Kx64 SBSRAM memory installed.

{*SDRAM_LEN_ID-1..0*}	R	Returns a capacity ID code for on-board SDRAM memory bank. {*SDRAM_LEN_ID-1..0*} = {0,0} setting corresponds to no SDRAM memory installed. {*SDRAM_LEN_ID-1..0*} = {0,1} setting corresponds to the 4Mx64 SDRAM memory installed. {*SDRAM_LEN_ID-1..0*} = {1,0} setting corresponds to the 16Mx64 SDRAM memory installed. {*SDRAM_LEN_ID-1..0*} = {1,1} setting is reserved.
{*DPRAM_LEN_ID-1..0*}	R	Returns a capacity ID code for on-board DPRAM memory bank and indicates whether the DPRAM memory provides dedicated memory locations for generation of the Host-to-DSP and DSP-to-Host interrupt requests. {*DPRAM_LEN_ID-1..0*} = {0,0} setting corresponds to no DPRAM memory installed. Although this value is valid, however it never appears in *TORNADO-P64xx* boards, which are not manufactured without the DPRAM memory installed. {*DPRAM_LEN_ID-1..0*} = {0,1} setting corresponds to the 128Kx32 DPSRAM memory installed. It is not possible to generate Host-to-DSP and DSP-to-Host interrupt requests via dedicated memory locations of the 128Kx32 DPRAM. { *DPRAM _LEN_ID-1..0*} = {1,0} setting corresponds to the 256Kx32 DPRAM memory installed. Note, that the 256Kx32 DPRAM supports generation of Host-to-DSP and DSP-to-Host interrupt requests via dedicated memory locations of DPRAM. {*DPRAM_LEN_ID-1..0*} = {1,1} setting corresponds to the 512Kx32 DPRAM memory installed. Note, that the 512Kx32 DPRAM supports generation of Host-to-DSP and DSP-to-Host interrupt requests via dedicated memory locations of DPRAM.

2.7 Updated firmware revision ID code in PCIC nvRAM memory

TORNADO-P64xx boards use the 8-bit memory location at address #23H of on-board PCIC nvRAM memory of host PCI-bus interface as the read-only ID code for the board firmware revision, which is used by host PC application in order to recognize the board firmware revision and to correspondingly configure the DSP on-chip EMIF registers for the DSP HPI bootmode and access to the DSP environment prior releasing the on-board DSP from the reset state.

Table 2-X3 below (this table is an add-on to *TORNADO-P64xx* User's Guide rev.4A) provides available settings of 8-bit nvRAM dataword at address #23H upon the firmware revision of *TORNADO-P64xx* board.

Table 2-X3. Firmware revision ID codes available via the address #23H of PCIC nvRAM dataword of *TORNADO-P64xx* boards.

register bit(s)	Access mode	Description
{*REV_ID-7..0*}	R	Returns a firmware revision ID code. {*REV_ID-7..0*} = {0,0,0,0,0,0,0,1} setting corresponds to initial firmware rev.1A of *TORNADO-P64xx* boards with 600MHz DSP (100MHz EMIF-A/B clock frequency). {*REV_ID-7..0*} = {0,0,0,0,0,0,1,0} setting corresponds to the firmware rev.1A-1 of *TORNADO-P64xx* boards with 600/720/1000MHz DSP (125MHz EMIF-A/B clock frequency). {*REV_ID-7..0*} = {0,0,0,0,0,0,1,1} setting corresponds to the firmware rev.1A-2 of *TORNADO-P64xx* boards with 600/720/1000MHz DSP (133MHz EMIF-A/B clock frequency). {*REV_ID-7..0*} = {0,0,0,0,0,1,0,0} setting corresponds to the firmware rev.1B of *TORNADO-P64xx* rev.1B boards with 600/720/1000MHz DSP (133MHz EMIF-A/B clock frequency). Other {*REV_ID-7..0*} codes are reserved for future expansion.

Notes: 1. The highlighted values correspond to the new settings available for *TORNADO-P64xx* boards with firmware rev.1A-1, rev.1A-2 and rev.1B.

2.8 Construction of *TORNADO-P64xx* rev.1B board

The hardware rev.1B of *TORNADO-P64xx* board (firmware rev.1B) has been released after release of *TORNADO-P64xx* User's Guide rev.4A, which covers the hardware rev.1A of *TORNADO-P64xx* board with firmware rev.1A only. This section provides details about construction of *TORNADO-P64xx* rev.1B board, which are the updates to section 2.1 and Appendix A of *TORNADO-P64xx* User's Guide rev.4A.

construction of TORNADO-P64xx rev.1B board

Figure 2-2d below (this figure is an add-on to *TORNADO-P64xx* User's Guide rev.4A) shows a construction of *TORNADO-P64xx* rev.1B board.

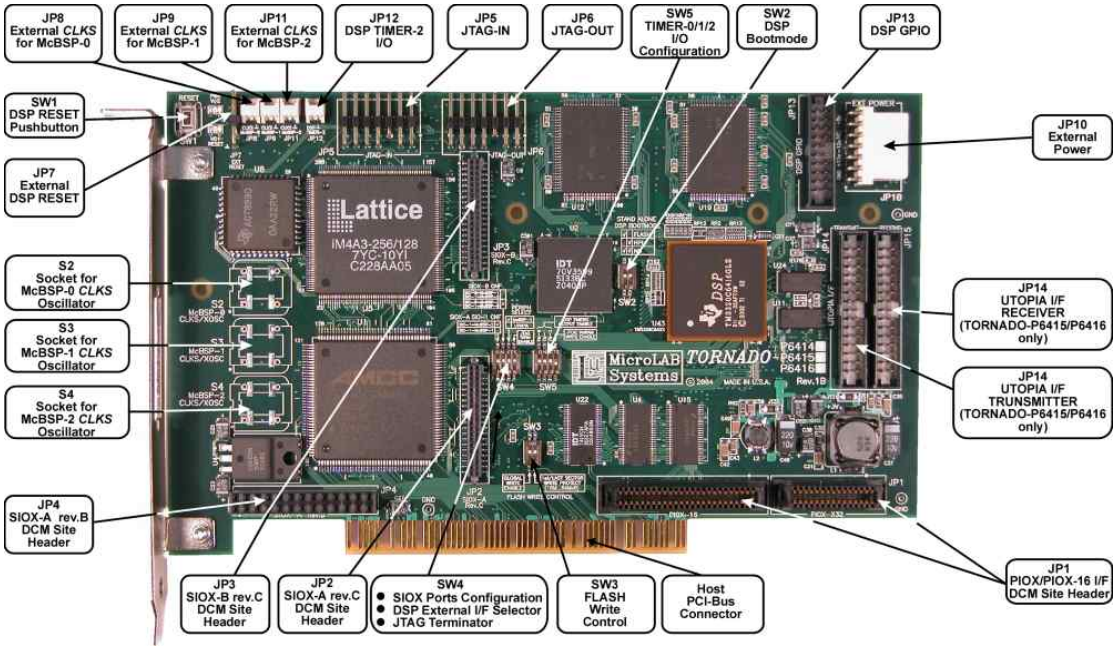

Fig.2-2d. Construction of *TORNADO-P6414/P6415/P6416* rev.1B board.

The following is the list of differences in constructions of new *TORNADO-P64xx* rev.1B board and of the *TORNADO-P64xx* rev.1A board, which is covered by *TORNADO-P64xx* User's Guide rev.4A:

- *TORNADO-PX64xxQ* rev.1B board provides the embedded (soldered-in) high-density FLASH memory with 512K..64Mx8 capacity instead of the on-board FLASH/EPROM PLCC-32 socket (S1) for plug-in either 512Kx8 FLASH or 1Mx8 EPROM memory at on *TORNADO-PX64xx* rev.1A board.
- *TORNADO-PX64xxQ* rev.1B provides a modified on-board SW3 switch, which is used for write protection control of on-board FLASH memory. Refer to section 2.9 for more details.
- *TORNADO-PX64xxQ* rev.1B provides the on-board SW5-4 switch, which is used for write protection control of on-board PCIC nvRAM. Refer to section 2.10 for more details.

construction of TORNADO-P64xx rev.1B board

Figure A-1d below (this figure is an add-on to *TORNADO-P64xx* User's Guide rev.4A) shows the on-board layout of configuration switches, connectors, sockets, and LED indicators for *TORNADO-P64xx* rev.1B board.

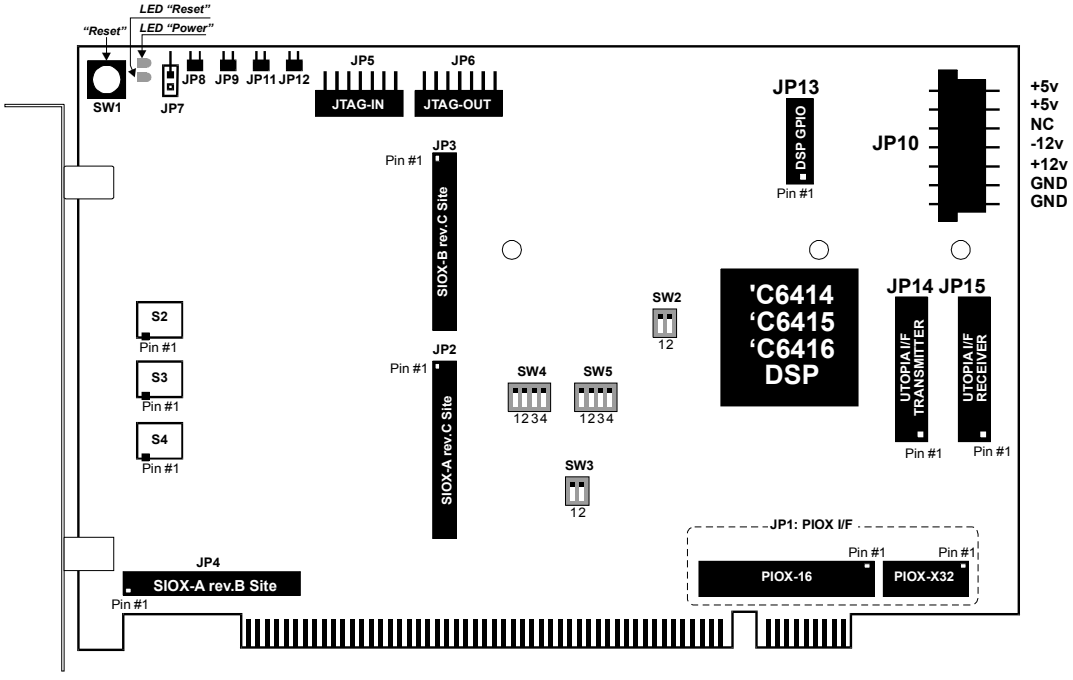

Fig.A-1d. On-board layout for *TORNADO-P64xx* rev.1B board.

on-board switches for TORNADO-P6x/P64xx boards

On-board switches for *TORNADO-P6x* DSP systems are listed in table [A-1], which is an update for the table A-1 from *TORNADO-P6x* User's Guide rev.4A.

Table [A-1]. On-board switches for *TORNADO-P6x*.

Switch ID	Switch function description	reference information
SW1	Reset pushbutton for TMS320C6x DSP stand-alone operation mode.	Section 2.2.
SW2	TMS320C6x DSP bootmode configuration. (*TORNADO-P6202/P6203/P64xx* only)	Section 2.2, tables 2-2a and 2-2b
SW3	FLASH/EPROM type selector. (*TORNADO-P6202/P6203* and *TORNADO-P64xx* rev.1A boards only)	Section 2.2 table 2-5

SW3-1	Global write enable for embedded FLASH memory. (*TORNADO-P64xx* rev.1A boards only)	Section 2.9 table 2-X5
SW3-2	1st/Last sector write protection enable for embedded FLASH memory. (*TORNADO-P64xx* rev.1A boards only)	Section 2.9 table 2-X6
SW4-1	SIO-1 port configuration for SIOX-A rev.B/C sites. (*TORNADO-P6202/P6203/P64xx* only)	Section 2.5 tables 2-27 and 2-29
SW4-2	SIO ports configuration for SIOX-B rev.C site. (*TORNADO-P6202/P6203/P64xx* only)	Section 2.5 tables 2-28 and 2-30
SW4-3	TMS320C6x DSP timer-0 IN/OUT configuration. (*TORNADO-P6202/P6203* only)	Sections 2.2, 2.4, 2.5 figure 2-4b
SW4-3	TMS320C6415/C6416 DSP external interface selector (*TORNADO-P6415/P6416* only)	Sections 2.2, 2.5 table 2-14
SW4-4	TMS320C6x DSP timer-1 IN/OUT configuration. (*TORNADO-P6202/P6203* only)	Sections 2.2, 2.4, 2.5 figure 2-4b
SW4-4	JTAG path terminator. (*TORNADO-P64xx* only)	Section 2.6
SW5-1	TMS320C6x DSP timer-0 IN/OUT configuration. (*TORNADO-P64xx* only)	Sections 2.2, 2.4, 2.5 figure 2-4c
SW5-2	TMS320C6x DSP timer-1 IN/OUT configuration. (*TORNADO-P64xx* only)	Sections 2.2, 2.4, 2.5 figure 2-4c
SW5-3	TMS320C6x DSP timer-2 IN/OUT configuration. (*TORNADO-P64xx* only)	Sections 2.2, 2.4, 2.5 figure 2-4c
SW5-4	PCIC nvRAM write enable. (*TORNADO-P64xx* rev.1B boards only)	Section 2.10 table 2-X7
SW6-1	JTAG path terminator enable. (*TORNADO-P6202/P6203* only)	Section 2.6

Notes: 1. The highlighted fields correspond to the new settings available for *TORNADO-P64xx* rev.1B boards.

on-board sockets for TORNADO-P6x/P64xx boards

On-board switches for *TORNADO-P6x* DSP systems are listed in table [A-4], which is an update for the table A-4 from *TORNADO-P6x* User's Guide rev.4A.

Table [A-4]. On-board sockets for *TORNADO-P6x/P64xx*.

socket ID	Socket function description	reference information
S1	PLCC-32 socket for FLASH/EPROM (5v power supply). (*TORNADO-P62/P67/P6202/P6203* and *TORNADO-P64xx* rev.1A boards only)	Section 2.2, 3.2 figure 3-1.
S2	DIP-8 socket for TTL/CMOS 5v crystal oscillator for external clock source of McBSP-0 serial port of TMS320C6x DSP.	Section 2.5 figures 2-18a, 2-18b, 2-18c
S3	DIP-8 socket for TTL/CMOS 5v crystal oscillator for external clock source of McBSP-1 serial port of TMS320C6x DSP.	Section 2.5 figures 2-18a, 2-18b, 2-18c
S4	DIP-8 socket for TTL/CMOS 5v crystal oscillator for external clock source of McBSP-2 serial port of TMS320C6x DSP. (*TORNADO-P6202/P6203/P64xx* only)	Section 2.5 figures 2-18b, 2-18c

Notes: 1. The highlighted table entry corresponds to the updated information including *TORNADO-P64xx* rev.1B boards.

on-board connectors and LED indicators for TORNADO-P6x/P64xx boards

On-board connectors and LED indicators for *TORNADO-P64xx* rev.1B boards remain the same as that for *TORNADO-P64xx* rev.1A boards and are listed in tables A-3 and A-5 correspondingly of *TORNADO-P6x* User's Guide rev.4A.

2.9 Embedded FLASH control at *TORNADO-P64xx* rev.1B board

TORNADO-PX64xxQ rev.1B board provides the embedded (soldered-in) high-density FLASH memory with 512K..64Mx8 capacity instead of the on-board FLASH/EPROM PLCC-32 socket (S1) for a plug-in either 512Kx8 FLASH or 1Mx8 EPROM memory at on *TORNADO-PX64xx* rev.1A board.

The on-board embedded high-density FLASH memory at *TORNADO-PX64xxQ* rev.1B board is mapped into the 8-bit EMIF-B CE1 external DSP memory space. Since the 8-bit EMIF-B CE-1 external DSP memory space has maximum 1Mx8 capacity, then the paging method is used to access the FLASH memory with capacity 2Mx8 and larger.

The following on-board and firmware resources are used to support the embedded FLASH control at *TORNADO-PX64xxQ* rev.1B boards:

- *DSP_XMEM2_LEN_ID_RG* DSP IOX register, which is used for identification of the on-board FLASH memory capacity
- *DSP_FLASH_PAGE_RG* DSP IOX register, which is used to select a 1Mx8 FLASH memory page, which is currently accessed (for FLASH capacity 2M..64Mx8 only).
- on-board SW3 switch, which is used for write protection control of on-board FLASH memory

The subsections below describe details about the on-board and firmware resources, which are used to support the embedded FLASH at *TORNADO-PX64xxQ* rev.1B boards.

embedded FLASH memory capacity for TORNADO-P64xx rev.1B board

Table 2-X4 below (this table is an add-on to *TORNADO-P64xx* User's Guide rev.4A) provides a list of all supported embedded FLASH memory capacities for *TORNADO-PX64xxQ* rev.1B board with the corresponding settings of the *FLASH_LEN_ID-0..3* field of the *DSP_XMEM2_LEN_ID_RG* DSP IOX register and number of bits in the *DSP_FLASH_PAGE_RG* DSP IOX register.

Table 2-X4. Embedded FLASH memory capacity for *TORNADO-P64xx* rev.1B boards.

FLASH capacity	**{*FLASH_LEN_ID-0..3*} bit field of the *DSP_XMEM2_LEN_ID_RG* DSP IOX register**	**Usage of the paging for FLASH access**	**Number of bits in the *DSP_FLASH_PAGE_RG* DSP IOX register**
Not installed	{0,0,0,0}	-	-
512Kx8	{0,0,0,1}	-	-
1Mx8	{0,0,1,0}	-	-
2Mx8	{0,0,1,1}	+	1
4Mx8	{0,1,0,0}	+	2
8Mx8	{0,1,0,1}	+	3
16Mx8	{0,1,1,0}	+	4
32Mx8	{0,1,1,1}	+	5
64Mx8	{1,0,0,0}	+	6

DSP_XMEM2_LEN_ID_RG IOX register

DSP_XMEM_LEN_ID_RG read-only DSP IOX register is used in *TORNADO-P64xx* rev.1B boards with firmware rev.1B in order to provide the ID code for on-board embedded FLASH memory capacity. Given that, user DSP application can recognize the capacity of on-board embedded FLASH memory capacity and to correspondingly configure the application variables.

DSP_XMEM2_LEN_ID_RG I/O control register (r)
(*TORNADO-P64xx* rev.1B board with firmware rev.1B)

X	*0*	*0*	*0*	*0*	*FLASH_ LEN_ID-1 (r)*	*FLASH_ LEN_ID-0 (r)*	*FLASH_ LEN_ID-1 (r)*	*FLASH_ LEN_ID-0 (r)*
bit-31...bit-8	Bit-7	bit-6	bit-5	Bit-4	bit-3	bit-2	bit-1	bit-0

The available values of the {*FLASH_LEN_ID-0..3*} bit field of the *DSP_XMEM_LEN_ID_RG* read-only DSP IOX register are listed in the table 2-X4.

NOTE

The *DSP_XMEM2_LEN_ID_RG* read-only DSP IOX register is not available in *TORNADO-P64xx* rev.1A boards with firmware rev.1A, rev.1A-1 and rev.1A-2.

DSP_FLASH_PAGE_RG IOX register

DSP_FLASH_PAGE_RG DSP IOX register is used in *TORNADO-P64xx* rev.1B boards with firmware rev.1B and 2Mx8 and larger capacities of on-board embedded FLASH memory installed in order to select the 1Mx8 FLASH memory page, which is currently accessed via the EMIF-B CE1 external DSP memory space.

The number of bits in *DSP_FLASH_PAGE_RG* DSP IOX register depends upon the capacity of on-board FLASH memory installed in accordance with the table 2-X4.

DSP_FLASH_PAGE_RG I/O control register (r/w)
(*TORNADO-P64xx* rev.1B board with firmware rev.1B)

X	*0*	*0*	*FLASH_PAGE-5* *(r/w, 0+)* *(FLASH capacity 64Mx8)* *0* *(r)* *(FLASH capacity ≤32Mx8)*	*FLASH_PAGE-4* *(r/w, 0+)* *(FLASH capacity ≥32Mx8)* *0* *(r)* *(FLASH capacity ≤16Mx8)*	*FLASH_PAGE-3* *(r/w, 0+)* *(FLASH capacity ≥16Mx8)* *0* *(r)* *(FLASH capacity ≤8Mx8)*	*FLASH_PAGE-2* *(r/w, 0+)* *(FLASH capacity ≥8Mx8)* *0* *(r)* *(FLASH capacity ≤4Mx8)*	*FLASH_PAGE-1* *(r/w, 0+)* *(FLASH capacity ≥4Mx8)* *0* *(r)* *(FLASH capacity ≤2Mx8)*	*FLASH_PAGE-0* *(r/w, 0+)* *(FLASH capacity ≥2Mx8)* *0* *(r)* *(FLASH capacity ≤1Mx8)*
bit-31...bit-8	Bit-7	bit-6	bit-5	Bit-4	bit-3	bit-2	bit-1	bit-0

NOTE

The *DSP_FLASH_PAGE_RG* DSP IOX register is not available in *TORNADO-P64xx* rev.1A boards with firmware rev.1A, rev.1A-1 and rev.1A-2.

On-board SW3-1 and SW3-2 switches for FLASH hardware write protection control at TORNADO-P64xx rev.1B boards

TORNADO-P64xx rev.1B board provides the on-board SW3-1 and SW3-2 switches, which are used for FLASH hardware write protection in order to guarantee safety of FLASH data contents.

The SW3-1 switch at *TORNADO-P64xx* rev.1B board is used to globally enable the FLASH write access, whereas the SW3-2 switch is used with 16M/32M/64Mx8 FLASH memories only in order to enable write protection for the 1st and last sector of the FLASH memory.

Tables 2-X5 and 2-X6 below (these tables are the add-on to *TORNADO-P64xx* User's Guide rev.4A) provide details about how to set the SW3-1 and SW3-2 switches at *TORNADO-P64xx* rev.1B board.

Table 2-X5. FLASH global write enable control via the SW3-1 switch at *TORNADO-P64xx* rev.1B board.

SW3-1 switch setting	Description
OFF	Writes to on-board FLASH memory are disabled.
ON	Writes to on-board FLASH memory are enabled.

Note: 1. Highlighted configuration corresponds to default factory setting.

Table 2-X6. FLASH 1st/last sector write protection control via the SW3-2 switch at *TORNADO-P64xx* rev.1B board.

SW3-2 switch setting	Description
OFF	Writes to the 1st/last sector of FLASH memory are enabled.
ON	Writes to the 1st/last sector of FLASH memory are disabled.

Note: 1. Highlighted configuration corresponds to default factory setting.

FLASH programming utilities

FLASH programming utilities for on-board embedded FLASH memory of *TORNADO-P64xx* rev.1B boards are included into the *TORNADO-P6x* DSP software utilities (*TP6X_DSP.H* file).

NOTE

TORNADO-P6x DSP software utilities (*TP6X_DSP.H* file) come standard with all *TORNADO-P6x* boards and are available for free download from MicroLAB Systems FTP site (ftp://ftp.mlabsys.com).

NOTE

In order to stay up-to-date with the latest FLASH memory programming utilities for *TORNADO-P64xx* rev.1B boards and firmware updates, and to minimize the software design efforts, it is recommended that user DSP applications for *TORNADO-P6x* boards are being designed using the latest release of *TORNADO-P6x* DSP software utilities, which come standard with all *TORNADO-P6x* boards and which are available from MicroLAB Systems FTP-site (ftp://ftp.mlabsys.com).

2.10 Write protection control for on-board PCIC nvRAM at *TORNADO-P64xx* rev.1B board

TORNADO-P64xx rev.1B board provides the on-board SW5-4 switch, which is used for hardware write protection for on-board PCIC nvRAM memory.

NOTE

Hardware write protection for on-board PCIC nvRAM memory is not available in *TORNADO-P64xx* rev.1A boards with firmware rev.1A, rev.1A-1 and rev.1A-2.

The on-board PCIC nvRAM memory contains important non-volatile information about host PCI-bus interface configuration of *TORNADO-P6x/P64xx* board, which must never be corrupted or overwritten in order to guarantee correct operation of host PCI-bus interface. However, on-board PCIC nvRAM at all *TORNADO-P620x/P67* boards and *TORNADO-P64xx* rev.1A boards does not provide hardware write protection and can generally be corrupted/overwritten by either host PC or DSP application, that may deliver a reliability problems for host PCI-bus interface operation. *TORNADO-P64xx* rev.1B board fixes this problem and provides hardware write protection for on-board PCIC nvRAM memory via the SW5-4 switch.

Table 2-X7 below (this table is an add-on to *TORNADO-P64xx* User's Guide rev.4A) provide details about how to set the SW5-4 switch at *TORNADO-P64xx* rev.1B board.

Table 2-X7. PCIC nvRAM write enable control via the SW5-4 switch at *TORNADO-P64xx* rev.1B board.

SW5-4 switch setting	Description
OFF	Writes to the PCIC nvRAM are disabled.
ON	Writes to the PCIC nvRAM are enabled.

Note: 1. Highlighted configuration corresponds to default factory setting.