# PCI Operation Registers 5

# CONTENTS

## 5.0 PCI BUS OPERATION REGISTERS

The PCI bus operation registers are mapped as 16 consecutive DWORD registers located at the address space (I/O or memory) specified by the Base Address Register 0 (Section 4.11). These locations are the primary method of communication between the PCI and Add-On buses. Data, software-defined commands and command parameters can be either exchanged through the mailboxes, transferred through the FIFO in blocks under program control, or transferred using the FIFOs under Bus Master control. Table 5-1 lists the PCI Bus Operation Registers.

***Table 5-1. Operation Registers — PCI Bus***

| Address Offset | Abbreviation | Register Name |
|---|---|---|
| 00h | OMB1 | Outgoing Mailbox Register 1 |
| 04h | OMB2 | Outgoing Mailbox Register 2 |
| 08h | OMB3 | Outgoing Mailbox Register 3 |
| 0Ch | OMB4 | Outgoing Mailbox Register 4 |
| 10h | IMB1 | Incoming Mailbox Register 1 |
| 14h | IMB2 | Incoming Mailbox Register 2 |
| 18h | IMB3 | Incoming Mailbox Register 3 |
| 1Ch | IMB4 | Incoming Mailbox Register 4 |
| 20h | FIFO | FIFO Register port (bidirectional) |
| 24h | MWAR | Master Write Address Register |
| 28h | MWTC | Master Write Transfer Count Register |
| 2Ch | MRAR | Master Read Address Register |
| 30h | MRTC | Master Read Transfer Count Register |
| 34h | MBEF | Mailbox Empty/Full Status |
| 38h | INTCSR | Interrupt Control/Status Register |
| 3Ch | MCSR | Bus Master Control/Status Register |

### 5.1 OUTGOING MAILBOX REGISTERS (OMB)

Register Names: Outgoing Mailboxes 1-4
PCI Address Offset: 00h, 04h, 08h, 0Ch
Power-up value: XXXXXXXXh
Attribute: Read/Write
Size: 32 bits

These four DWORD registers provide a method for sending command or parameter data to the Add-On system. PCI bus operations to these registers may be in any width (byte, word, or DWORD). Writing to these registers can be a source for Add-On bus interrupts (if desired) by enabling their interrupt generation through the use of the Add-On's interrupt control/status register (Section 6.9).

### 5.2 INCOMING MAILBOX REGISTERS (IMB)

Register Names: Incoming Mailboxes 1-4
PCI Address Offset: 10h, 14h, 18h, 1Ch
Power-up value: XXXXXXXXh
Attribute: Read Only
Size: 32 bits

These four DWORD registers provide a method for receiving user defined data from the Add-On system. PCI bus read operations to these registers may be in any width (byte, word, or DWORD). Only read operations are supported. Reading from these registers can optionally cause an Add-On bus interrupt (if desired) by enabling their interrupt generation through the use of the Add-On's interrupt control/status register (described in Section 6.9).

Mailbox 4, byte 3 only exists as device pins on the S5933 devices when used with a serial nonvolatile memory.

### 5.3 FIFO REGISTER PORT (FIFO)

Register Name: FIFO Port
PCI Address Offset: 20h
Power-up value: XXXXXXXXh
Attribute: Read/Write
Size: 32 bits

This location provides access to the bidirectional FIFO. Separate registers are used when reading from or writing to the FIFO. Accordingly, it is not possible to read what was written to this location. The FIFO registers are implicitly involved in all bus master operations and, as such, should not be accessed during active bus master transfers. When operating upon the FIFOs with software program transfers involving word or byte operations, the *endian* sequence of the FIFO should be established as outlined in Section 11.1.1.2 in order to preserve the internal FIFO data ordering and flag management. The FIFO's fullness may be observed by reading the master control-status register, MCSR, described in Section 5.10.

### 5.4 PCI CONTROLLED BUS MASTER WRITE ADDRESS REGISTER (MWAR)

Register Name: Master Write Address
PCI Address Offset: 24h
Power-up value: 00000000h
Attribute: Read/Write
Size: 32 bits

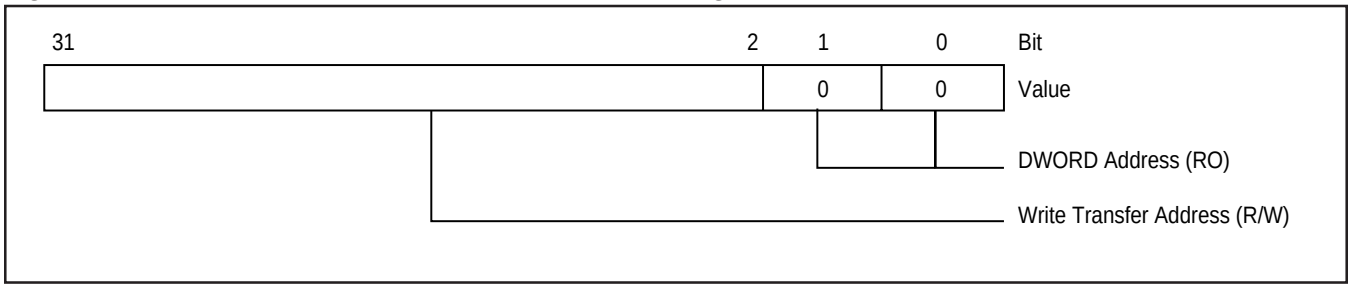
This register is used to establish the PCI address for data moving from the Add-On bus to the PCI bus during PCI bus memory write operations. It consists of a 30-bit counter with the low-order two bits hardwired as zeros. Transfers may be any non-zero byte length as defined by the transfer count register, MWTC (Section 5.5), and must begin on a DWORD boundary. This DWORD boundary starting constraint is placed upon this controller's PCI bus master transfers so that byte lane alignment can be maintained between the S5933 controller's internal FIFO data path, the Add-On interface, and the PCI bus.

Note: Applications which require a non-DWORD starting boundary will need to move the first few bytes under software program control (and without using the FIFO) to establish a DWORD boundary. After the DWORD boundary is established the S5933 can begin the task of PCI bus master data transfers.

The Master Write Address Register is continually updated during the transfer process and will always be pointing to the next unwritten location. Reading of this register during a transfer process (done when the S5933 controller is functioning as a target, i.e. not a bus master) is permitted and may be used to monitor the progress of the transfer. During the address phase for bus master write transfers, the two least significant bits presented on the PCI bus pins AD[31:0] will always be zero. This identifies to the target memory that the burst address sequence will be in a linear order rather than in an Intel 486 or Pentium™ cache line fill sequence. Also, the PCI bus address bit A1 will always be zero when this controller is the bus master. This signifies to the target that the S5933 controller is burst capable and that the target should not arbitrarily disconnect after the first data phase of this operation.

Under certain circumstances, MWAR can be accessed from the Add-On bus instead of the PCI bus. See Section 11.1.4.1.

***Figure 5-1. PCI Controlled Bus Master Write Address Register***



### 5.5 PCI CONTROLLED BUS MASTER WRITE TRANSFER COUNT REGISTER (MWTC)

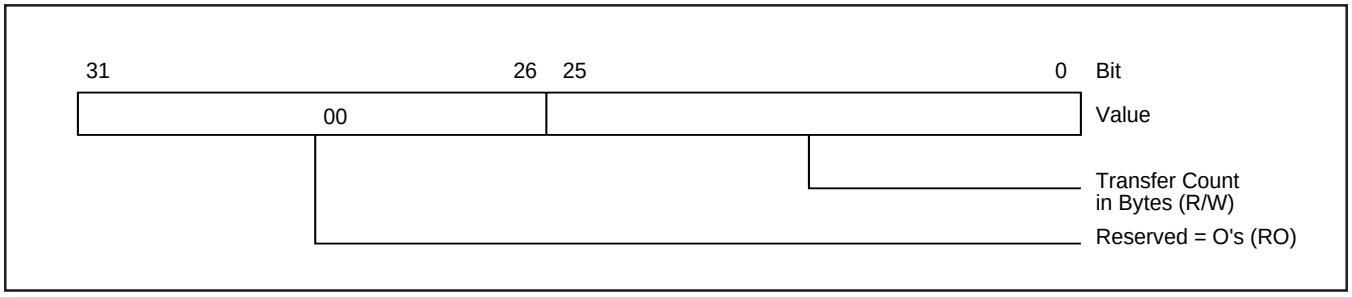
Register Name: Master Write Transfer Count
PCI Address Offset: 28h
Power-up value: 00000000h
Attribute: Read/Write
Size: 32 bits

The master write transfer count register is used to convey to the S5933 controller the actual number of bytes that are to be transferred. The value in this register is decremented with each bus master PCI write operation until the transfer count reaches zero.

Upon reaching zero, the transfer operation ceases and an interrupt may be optionally generated to either the PCI or Add-On bus interface. Transfers which are not whole multiples of DWORDs in size result in a partial word ending cycle. This partial word ending cycle is possible since all bus master transfers for this controller are required to begin on a DWORD boundary.

Under certain circumstances, MWTC can be accessed from the Add-On bus instead of the PCI bus. See Section 11.1.4.1.

***Figure 5-2. PCI Controlled Bus Master Write Transfer Count Register***



### 5.6 PCI CONTROLLED BUS MASTER READ ADDRESS REGISTER (MRAR)

Register Name: Master Read Address
PCI Address Offset: 2Ch
Power-up value: 00000000h
Attribute: Read/Write
Size: 32 bits

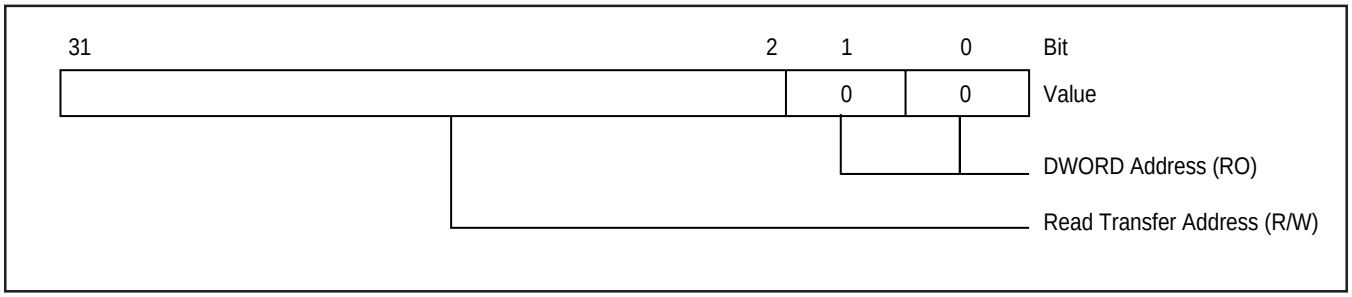
This register is used to establish the PCI address for data moving to the Add-On bus from the PCI bus during PCI bus memory read operations. It consists of a 30-bit counter with the low-order two bits hardwired as zeros. Transfers may be any non-zero byte length as defined by the transfer count register, MRTC (Section 5.7) and must begin on a DWORD boundary. This DWORD boundary starting constraint is placed upon this controller's PCI bus master transfers so that byte lane alignment can be maintained between the S5933 controller's internal FIFO data path, the Add-On interface and the PCI bus.

Note: Applications which require a non-DWORD starting boundary will need to move the first few bytes under software program control (and without using the FIFO) to establish a DWORD boundary. After the DWORD boundary is established the S5933 can begin the task of PCI bus master data transfers.

The Master Read Address Register is continually updated during the transfer process and will always be pointing to the next unread location. Reading of this register during a transfer process (done when the S5933 controller is functioning as a target—i.e., not a bus master) is permitted and may be used to monitor the progress of the transfer. During the address phase for bus master read transfers, the two least significant bits presented on the PCI bus AD[31:0] will always be zero. This identifies to the target memory that the burst address sequence will be in a linear order rather than in an Intel 486 or Pentium™ cache line fill sequence. Also, the PCI bus address bit A1 will always be zero when this controller is the bus master. This signifies to the target that the controller is burst capable and that the target should not arbitrarily disconnect after the first data phase of this operation.

Under certain circumstances, MRAR can be accessed from the Add-On bus instead of the PCI bus. See Section 11.1.4.1.

***Figure 5-3. PCI Controlled Bus Master Read Address Register***



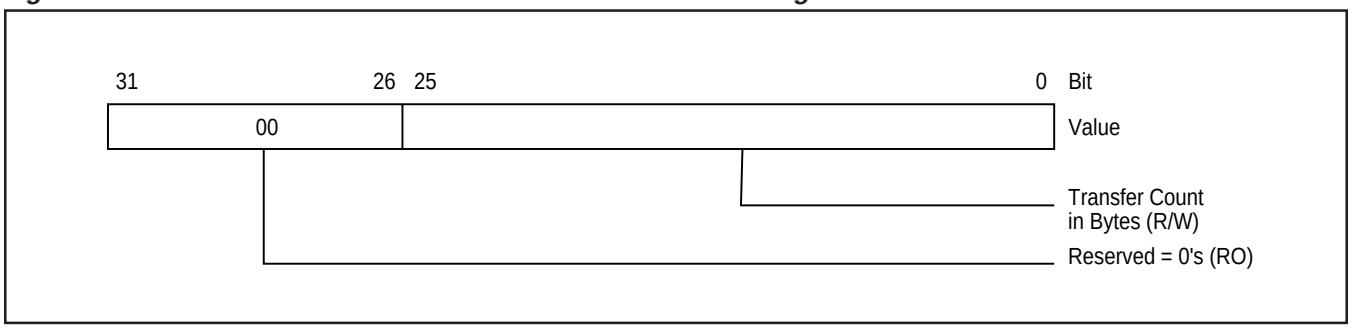
### 5.7 PCI CONTROLLED BUS MASTER READ TRANSFER COUNT REGISTER (MRTC)

Register Name: Master Read Transfer Count
PCI Address Offset: 30h
Power-up value: 00000000h
Attribute: Read/Write
Size: 32 bits

The master read transfer count register is used to convey to the PCI controller the actual number of bytes that are to be transferred. The value in this register is decremented with each bus master PCI read operation until the transfer count reaches zero. Upon reaching zero, the transfer operation ceases and an interrupt may be optionally generated to either the PCI or Add-On bus interface. Transfers which are not whole multiples of DWORDs in size result in a partial word ending cycle. This partial word ending cycle is possible since all bus master transfers for this controller are required to begin on a DWORD boundary.

Under certain circumstances, MRTC can be accessed from the Add-On bus instead of the PCI bus. See Section 11.1.4.1.

***Figure 5-4. PCI Controlled Bus Master Read Transfer Count Register***



### 5.8 MAILBOX EMPTY FULL/STATUS REGISTER (MBEF)

Register Name: Mailbox Empty/Full Status

PCI Address Offset: 34h

Power-up value: 00000000h

Attribute: Read Only

Size: 32 bits

This register provides empty/full visibility of each byte within the mailboxes. The empty/full status for the Outgoing mailboxes is displayed on the low-order 16 bits and the empty/full status for the Incoming mailboxes is presented on the high-order 16 bits. A value of 1 signifies that a given mailbox has been written by one bus interface but has not yet been read by the corresponding destination interface. A PCI bus incoming mailbox is defined as one in which data travels from the Add-On bus into the PCI bus, and an outgoing mailbox is defined as one where data travels out from the PCI bus to the Add-On interface.

***Figure 5-5. Mailbox Empty/Full Status Register***

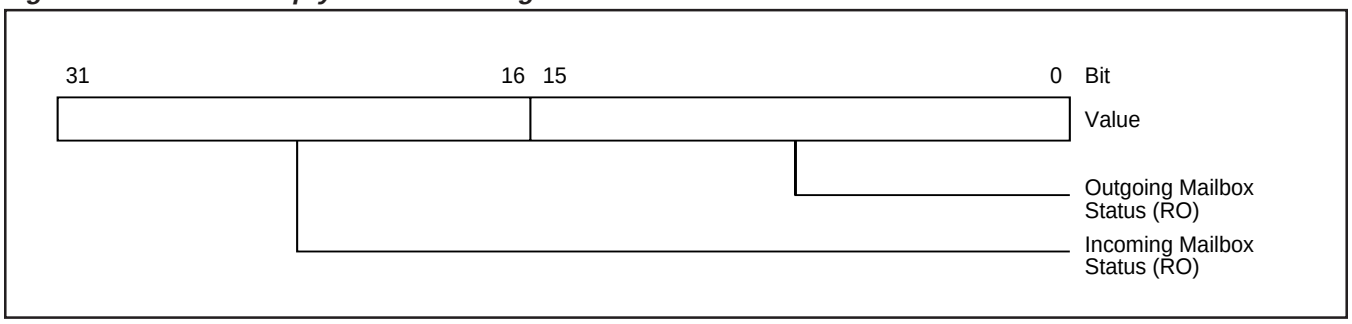


***Table 5-2. Mailbox Empty/Full Status Register***

| Bit | Description |
|---|---|
| 31:16 | Incoming Mailbox Status. This field indicates which incoming mailbox registers have been written by the Add-On interface but have not yet been read by the PCI bus. Each bit location corresponds to a specific byte within one of the four incoming mailboxes. A value of one for each bit signifies that the specified mailbox byte is full, and a value of zero signifies empty. The mapping of these status bits to bytes within each mailbox is as follows:<br>Bit 31 = Incoming mailbox 4 byte 3<br>Bit 30 = Incoming mailbox 4 byte 2<br>Bit 29 = Incoming mailbox 4 byte 1<br>Bit 28 = Incoming mailbox 4 byte 0<br>Bit 27 = Incoming mailbox 3 byte 3<br>Bit 26 = Incoming mailbox 3 byte 2<br>Bit 25 = Incoming mailbox 3 byte 1<br>Bit 24 = Incoming mailbox 3 byte 0<br>Bit 23 = Incoming mailbox 2 byte 3<br>Bit 22 = Incoming mailbox 2 byte 2<br>Bit 21 = Incoming mailbox 2 byte 1<br>Bit 20 = Incoming mailbox 2 byte 0<br>Bit 19 = Incoming mailbox 1 byte 3<br>Bit 18 = Incoming mailbox 1 byte 2<br>Bit 17 = Incoming mailbox 1 byte 1<br>Bit 16 = Incoming mailbox 1 byte 0 |
| 15:00 | Outgoing Mailbox Status. This field indicates which out going mail box registers have been written by the PCI bus interface but have not yet been read by the Add-On bus. Each bit location corresponds to a specific byte within one of the four outgoing mailboxes. A value of one for each bit signifies that the specified mailbox byte is full, and a value of zero signifies empty. The mapping of these status bits to bytes within each mailbox is as follows:<br>Bit 15 = Outgoing mailbox 4 byte 3<br>Bit 14 = Outgoing mailbox 4 byte 2<br>Bit 13 = Outgoing mailbox 4 byte 1<br>Bit 12 = Outgoing mailbox 4 byte 0<br>Bit 11 = Outgoing mailbox 3 byte 3<br>Bit 10 = Outgoing mailbox 3 byte 2<br>Bit 09 = Outgoing mailbox 3 byte 1<br>Bit 08 = Outgoing mailbox 3 byte 0<br>Bit 07 = Outgoing mailbox 2 byte 3<br>Bit 06 = Outgoing mailbox 2 byte 2<br>Bit 05 = Outgoing mailbox 2 byte 1<br>Bit 04 = Outgoing Mailbox 2 byte 0<br>Bit 03 = Outgoing Mailbox 1 byte 3<br>Bit 02 = Outgoing Mailbox 1 byte 2<br>Bit 01 = Outgoing Mailbox 1 byte 1<br>Bit 00 = Outgoing Mailbox 1 byte 0 |

### 5.9 INTERRUPT CONTROL/STATUS REGISTER (INTCSR)

Register Name: Interrupt Control and Status
PCI Address Offset: 38h
Power-up value: 00000000h
Attribute: Read/Write (R/W), Read/Write_One_Clear (R/WC)
Size: 32 bits

This register provides the method for choosing which conditions are to produce an interrupt on the PCI bus interface, a method for viewing the cause of the interrupt, and a method for acknowledging (removing) the interrupt's assertion.

Interrupt sources:

- Write Transfer Terminal Count = zero
- Read Transfer Terminal Count = zero
- One of the Outgoing mailboxes (1,2,3 or 4) becomes empty
- One of the Incoming mailboxes (1,2,3 or 4) becomes full.
- Target Abort
- Master Abort

***Figure 5-6. Interrupt Control/Status Register***

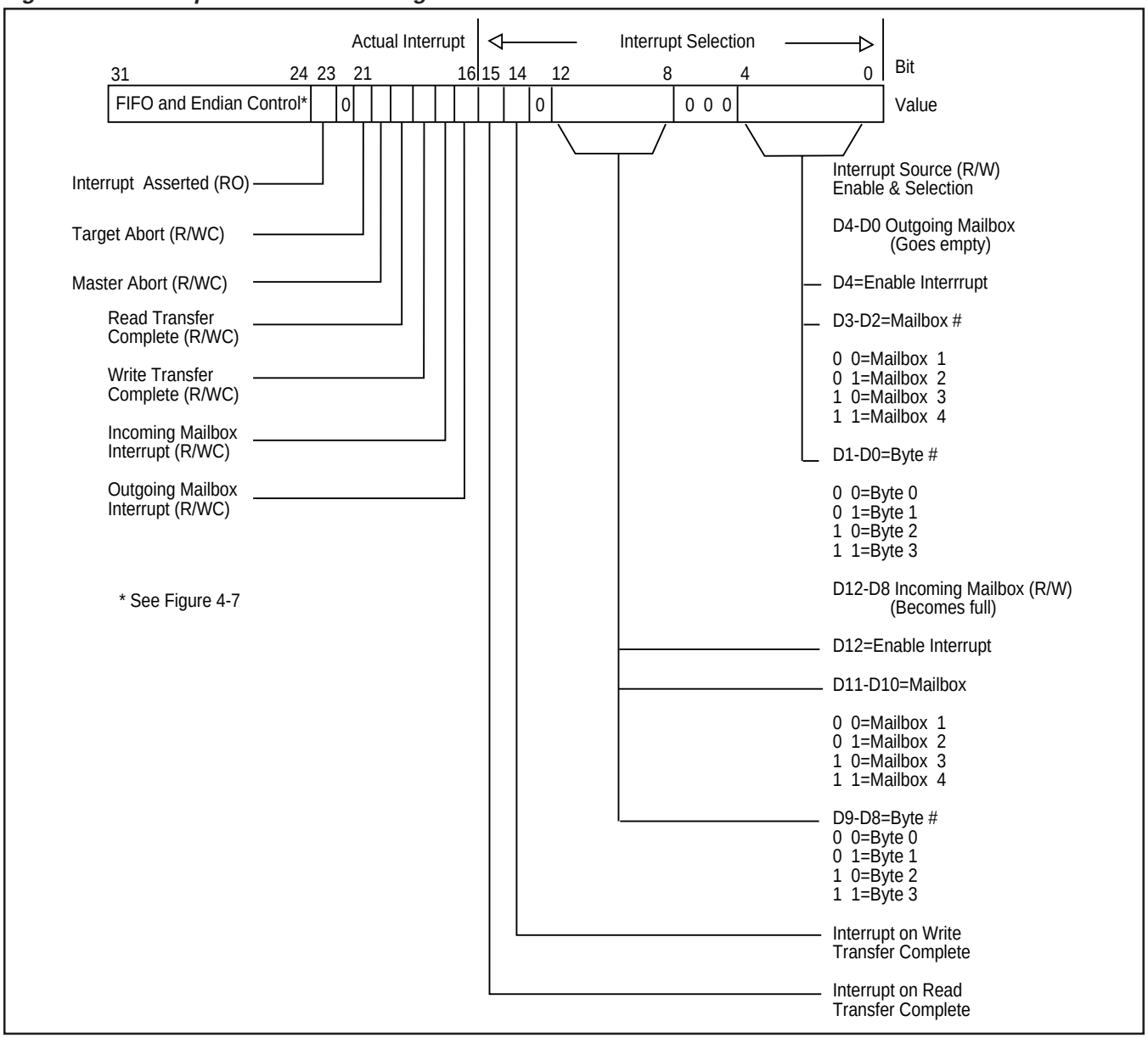


***Figure 5-7. FIFO Management and Endian Control Byte***

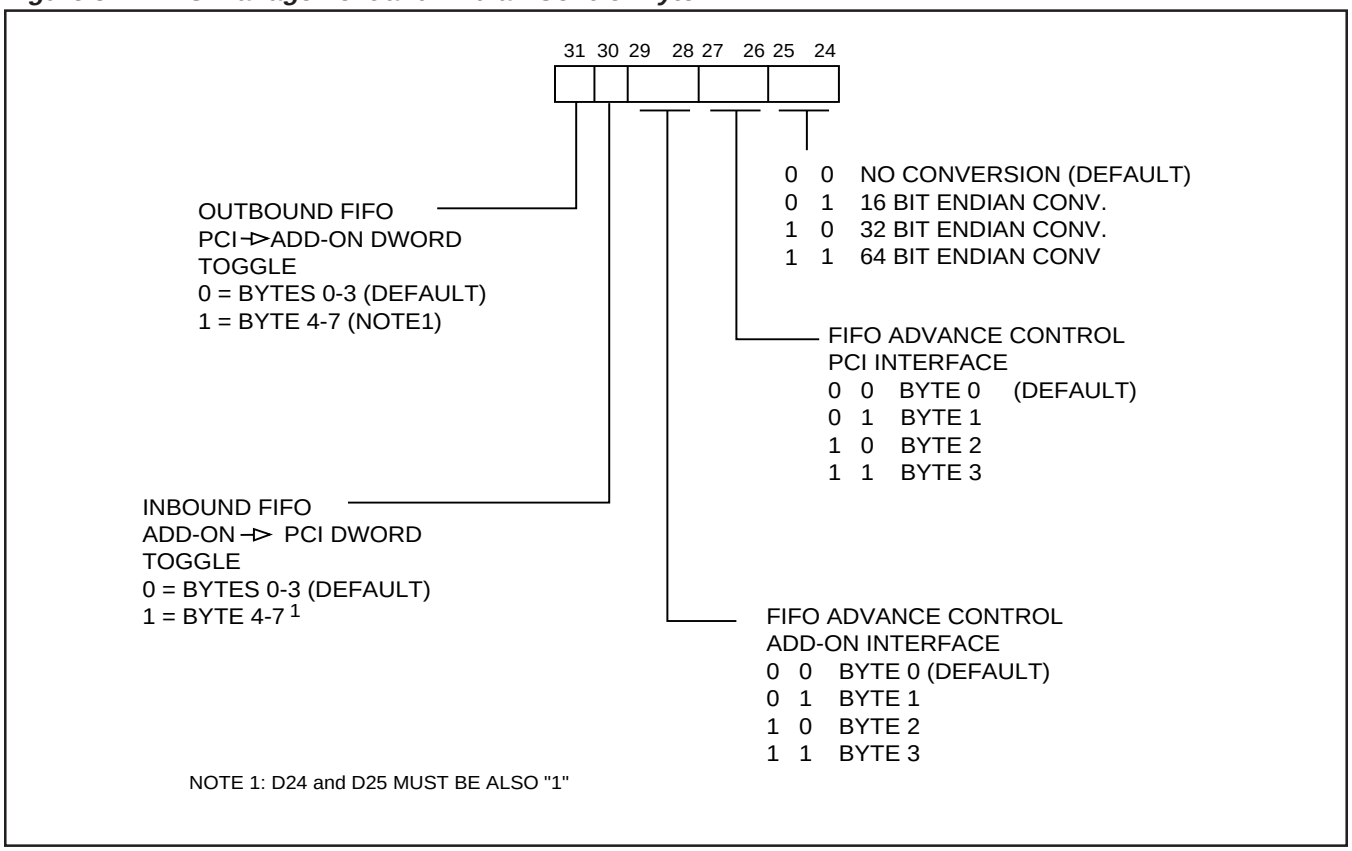


***Table 5-3. Interrupt Control/Status Register***

| Bit | Description |
|---|---|
| 31:24 | FIFO and Endian Control (see Section 11.1.1). |
| 23 | Interrupt asserted. This read only status bit indicates that one or more of the four possible interrupt conditions is present. This bit is nothing more than the ORing of the interrupt conditions described by bits 19 through 16 of this register. |
| 22 | Reserved. Always zero. |
| 21 | Target Abort. This bit signifies that an interrupt has been generated due to the S5933 encountering a target abort during a PCI bus cycle while the S5933 was the current bus master. This bit operates as read or write one clear. A write to this bit with the data of “one” will cause this bit to be reset, a write to this bit with the data of “zero” will not change the state of this bit. |
| 20 | Master Abort. This bit signifies that an interrupt has been generated due to the S5933 encountering a Master Abort on the PCI bus. A master abort occurs when there is no target response to a PCI bus cycle (see Section 8.1.4.3). This bit operates as read or write one clear. A write to this bit with the data of “one” will cause this bit be reset, a write to this bit with the data of “zero” will not change the state of this bit. |
| 19 | Read Transfer Complete. This bit signifies that an interrupt has been generated due to the completion of a PCI bus master operation involving the transfer of data from the PCI bus to the Add-On. This interrupt will occur when the Master Read Transfer Count register reaches zero. This bit operates as read or write one clear. A write to this bit with the data of “one” will cause this bit to be reset; a write to this bit with the data of “zero” will not change the state of this bit. |
| 18 | Write Transfer Complete. This bit signifies that an interrupt has been generated due to the completion of a PCI bus master operation involving the transfer of data to the PCI bus from the Add-On. This interrupt will occur when the Master Write Transfer Count register reaches zero. This bit operates as read or write one clear. A write to this bit with the data of “one” will cause this bit to be reset; a write to this bit with the data of “zero” will not change the state of this bit. |
| 17 | Incoming Mailbox Interrupt. This bit is set when the mailbox selected by bits 12 through 8 of this register are written by the Add-On interface. This bit operates as read or write one clear. A write to this bit with the data of “one” will cause this bit to be reset; a write to this bit with the data as “zero” will not change the state of this bit. |
| 16 | Outgoing Mailbox Interrupt. This bit is set when the mailbox selected by bits 4 through 0 of this register is read by the Add-On interface. This bit operates as read or write one clear. A write to this bit with the data of “one” will cause this bit to be reset; a write to this bit with the data of “zero” will not change the state of this bit. |
| 15 | Interrupt on Read Transfer Complete. This bit enables the occurrence of an interrupt when the read transfer count reaches zero. This bit is read/write. |
| 14 | Interrupt on Write Transfer Complete. This bit enables the occurrence of an interrupt when the write transfer count reaches zero. This bit is read/write. |
| 13 | Reserved. Always zero. |
| 12 | Enable incoming mailbox interrupt. This bit allows a write from the incoming mailbox register identified by bits 11 through 8 to produce a PCI interface interrupt. This bit is read/write. |
| 11:10 | Incoming Mailbox Interrupt Select. This field selects which of the four incoming mailboxes is to be the source for causing an incoming mailbox interrupt. [00]b selects mailbox 1, [01]b selects mailbox 2, [10]b selects mailbox 3 and [11]b selects mailbox 4. This field is read/write. |

***Table 5-3. Interrupt Control/Status Register (Continued)***

| Bit | Description |
|---|---|
| 9:8 | Incoming Mailbox Byte Interrupt select. This field selects which byte of the mailbox selected by bits 10 and 11 above is to actually cause the interrupt. [00]b selects byte 0, [01]b selects byte 1, [10]b selects byte 2, and [11]b selects byte 3. This field is read/write. |
| 7:5 | Reserved, Always zero. |
| 4 | Enable outgoing mailbox interrupt. This bit allows a read by the Add-On of the outgoing mailbox register identified by bits 3 through 0 to produce a PCI interface interrupt. This bit is read/write. |
| 3:2 | Outgoing Mailbox Interrupt Select. This field selects which of the four outgoing mailboxes is to be the source for causing an outgoing mailbox interrupt. [00]b selects mailbox 1, [01]b selects mailbox 2, [10]b selects mailbox 3 and [11]b selects mailbox 4. This field is read/write. |
| 1:0 | Outgoing Mailbox Byte Interrupt select. This field selects which byte of the mailbox selected by bits 3 and 2 above is to actually cause the interrupt. [00]b selects byte 0, [01]b selects byte 1, [10]b selects byte 2, and [11]b selects byte 3. This field is read/write. |

### 5.10 MASTER CONTROL/STATUS REGISTER (MCSR)

Register Name: Master Control/Status
PCI Address Offset: 3Ch
Power-up value: 000000E6h
Attribute: Read/Write, Read Only, Write Only
Size: 32 bits

This register provides for overall control of this device. It is used to enable bus mastering for both data directions as well as providing a method to perform software resets.

The following PCI bus controls are available:

- Write Priority over Read
- Read Priority over Write
- Write Transfer Enable
- Write master requests on 4 or more FIFO words available (full)
- Read transfer enable
- Read master requests on 4 or more FIFO available (empty)
- Assert reset to Add-On
- Reset Add-On to PCI FIFO flags
- Reset PCI to Add-On FIFO flags
- Reset mailbox empty full status flags
- Write external non-volatile memory

The following PCI interface status flags are provided:

- PCI to Add-On FIFO FULL
- PCI to Add-On FIFO has four or more empty locations
- PCI to Add-On FIFO EMPTY
- Add-On to PCI FIFO FULL
- Add-On to PCI FIFO has four or more words loaded
- Add-On to PCI FIFO EMPTY
- PCI to Add-On Transfer Count = Zero
- Add-On to PCI Transfer Count = Zero

***Figure 5-8. Bus Master Control/Status Register***

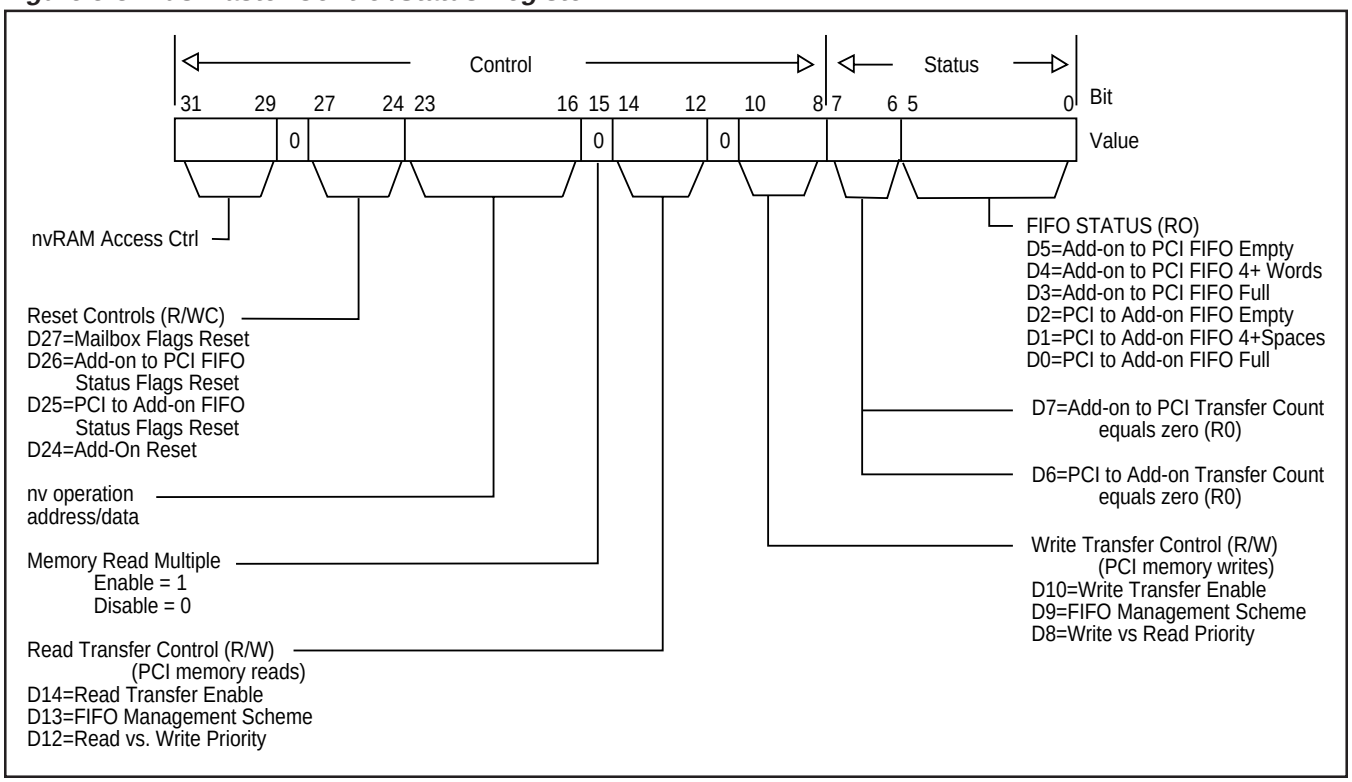


***Table 5-4. Bus Master Control/Status Register***

| Bit | Description |
|---|---|
| 31:29 | nvRAM Access Control. This field provides a method for access to the optional external non-volatile memory. Write operations are achieved by a sequence of byte operations involving these bits and the 8-bit field of bits 23 through 16. The sequence requires that the low-order address, high order address, and then a data byte are loaded in order. Bit 31 of this field acts as a combined enable and ready for the access to the external memory. D31 must be written to a 1 before an access can begin, and subsequent accesses must wait for bit D31 to become zero (ready).<br><br>D31 D30 D29 W/R<br>0 X X W Inactive<br>1 0 0 W Load low address byte<br>1 0 1 W Load high address byte<br>1 1 0 W Begin write<br>1 1 1 W Begin read<br>0 X X R Ready<br>1 X X R Busy<br><br>Cautionary note: The nonvolatile memory interface is also available for access by the Add-On interface. Accesses by both the Add-On and PCI bus to the nv memory are not directly supported by the S5933 device. Software must be designed to prevent the simultaneous access of nv memory to prevent data corruption within the memory and provide for accurate data retrieval. |
| 28 | FIFO loop back mode. |
| 27 | Mailbox Flag Reset. Writing a one to this bit causes all mailbox status flags to become reset (EMPTY). It is not necessary to write this bit as zero because it is used internally to produce a reset pulse. Since reading of this bit will always produce zeros, this bit is write only. |
| 26 | Add-On to PCI FIFO Status Reset. Writing a one to this bit causes the Add-On to PCI (Bus master memory writes) FIFO empty flag to set indicating empty and the FIFO FULL flag to reset and the FIFO Four Plus word flag to reset. It is not necessary to write this bit as zero because it is used internally to produce a reset pulse. Since reading of this bit will always produce zeros, this bit is write only. |
| 25 | PCI to Add-On FIFO Status Reset. Writing a one to this bit causes the PCI to Add-On (Bus master memory reads) FIFO empty flag to set indicating empty and the FIFO FULL flag to reset and the FIFO Four Plus words available flag to set. It is not necessary to write this bit as zero because it is used internally to produce a reset pulse. Since reading of this bit will always produce zeros, this bit is write only. |
| 24 | Add-On pin reset. Writing a one to this bit causes the reset output pin to become active. Writing a zero to this pin is necessary to remove the assertion of reset. This register bit is read/write. |
| 23:16 | Non-volatile memory address/data port. This 8-bit field is used in conjunction with bit 31, 30 and 29 of this register to access the external non-volatile memory. The contents written are either low address, high address, or data as defined by bits 30 and 29. This register will contain the external non-volatile memory data when the proper read sequence for bits 31 through 29 is performed. |

***Table 5-4. Bus Master Control/Status Register (Continued)***

| Bit | Description |
|---|---|
| 15 | Enable memory read multiple during S5933 bus mastering mode. |
| 14 | Read Transfer Enable. This bit must be set to a one for S5933 PCI bus master read transfers to take place. Writing a zero to this location will suspend an active transfer. An active transfer is one in which the transfer count is not zero. |
| 13 | Read FIFO management scheme. When set to a 1, this bit causes the controller to refrain from requesting the PCI bus unless it has four or more vacant FIFO locations to fill. Once the controller is granted the PCI bus or is in possession of the bus due to the write channel, this constraint is not meaningful. When this bit is zero the controller will request the PCI bus if it has at least one vacant FIFO word. |
| 12 | Read versus Write priority. This bit controls the priority of read transfers over write transfers. When set to a 1 with bit D8 as zero this indicates that read transfers always have priority over write transfers; when set to a one with D8 as one, this indicates that transfer priorities will alternate equally between read and writes. |
| 11 | Reserved. Always zero. |
| 10 | Write Transfer Enable. This bit must be set to a one for PCI bus master write transfers to take place. Writing a zero to this location will suspend an active transfer. An active transfer is one in which the transfer count is not zero. |
| 9 | Write FIFO management scheme. When set to a one this bit causes the controller to refrain from requesting the PCI bus unless it has four or more FIFO locations filled. Once the S5933 controller is granted the PCI bus or is in possession of the bus due to the write channel, this constraint is not meaningful. When this bit is zero the controller will request the PCI bus if it has at least one valid FIFO word. |
| 8 | Write versus Read priority. This bit controls the priority of write transfers over read transfers. When set to a one with bit D12 as zero this indicates that write transfers always have priority over read transfers; when set to a one with D12 as one, this indicates that transfer priorities will alternate equally between writes and reads. |
| 7 | Add-On to PCI Transfer Count Equal Zero (RO). This bit is a one to signify that the write transfer count is all zeros. |
| 6 | PCI to Add-On Transfer Count Equals Zero (RO). This bit is a one to signify that the read transfer count is all zeros. |
| 5 | Add-On to PCI FIFO Empty. This bit is a one when the Add-On to PCI bus FIFO is completely empty. |
| 4 | Add-On to PCI 4+ words. This bit is a one when there are four or more FIFO words valid within the Add-On to PCI bus FIFO. |
| 3 | Add-On to PCI FIFO Full. This bit is a one when the Add-On to PCI bus FIFO is completely full. |
| 2 | PCI to Add-On FIFO Empty. This bit is a one when the PCI bus to Add-On FIFO is completely empty. |
| 1 | PCI to Add-On FIFO 4+ spaces. This bit signifies that there are at least four empty words within the PCI to Add-On FIFO. |
| 0 | PCI to Add-On FIFO Full. This bit is a one when the PCI bus to Add-On FIFO is completely full. |