MicroLAB Systems

Ultimate DSP Development Solutions

DIGITAL SIGNAL PROCESSING

TORNADO-P6x

Ultra-High Performance 32-bit Fixed/Floating-Point TMS320C6x DSP Systems
for Host PCI-bus Computers and Stand-alone Applications

User's Guide

covers:
TORNADO-P62/P67 rev.2B
TORNADO-P6202/P6203 rev.1C
TORNADO-P6414/P6415/P6416 rev.1A

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About this Document

This user's guide contains description for *TORNADO-P62/P67* rev.2B and *TORNADO-P6202/P6203* rev.1C ultra-high performance 32-bit fixed- and floating-point digital signal processing (DSP) systems for PCI-bus host computers and stand-alone applications, which utilize TMS320C6x DSP from Texas Instruments Inc (TI).

This document does not include detail description neither for TI TMS320C6x DSP nor for the corresponding software and hardware applications. To get the corresponding information please refer to the following documentation:

1. ***TMS320C6x Peripheral Reference Guide.*** Texas Instruments Inc, SPRU190D, USA, 2001.
2. ***TMS320C6x CPU and Instruction Set Reference Guide.*** Texas Instruments Inc, SPRU189F, USA, 2000.
3. ***TMS320C6x Programmer's Guide.*** Texas Instruments Inc, SPRU198D, USA, 2000.
4. ***TMS320C6x Optimizing C Compiler User`s Guide.*** Texas Instruments Inc, SPRU187C, USA, 1998.
5. ***TMS320C6x Assembly Language Tools User`s Guide.*** Texas Instruments Inc, SPRU186C, USA, 1998.
6. ***S5933 PCI Controller Databook.*** AMCC, 1997.

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Chapter 1. Introduction

This chapter contains general description for *TORNADO-P6x* DSP systems product line, which comprises of *TORNADO-P62*, *TORNADO-P67*, *TORNADO-P6202*, *TORNADO-P6203*, *TORNADO-P6414*, *TORNADO-P6415*, and *TORNADO-P6416* DSP systems.

TORNADO-P6x DSP systems are designed to accommodate either 32-bit fixed-point TMS320C6201/C6202/C6203/C6414/C6415/C6416 DSP or compatible 32-bit floating-point TMS320C6701 DSP from TI.

CAUTION

The particular DSP installed specifies the final name of *TORNADO-P6x* DSP system, i.e. *TORNADO-P62* (with TMS320C6201 DSP), *TORNADO-P67* (with TMS320C6701 DSP), *TORNADO-P6202* (with TMS320C6202 DSP), or *TORNADO-P6203* (with TMS320C6203 DSP), or *TORNADO-P6414* (with TMS320C6414 DSP), or *TORNADO-P6415* (with TMS320C6415 DSP), or *TORNADO-P6416* (with TMS320C6416 DSP).

CAUTION

'*TORNADO-P6x*' notation denotes that the supplied information is applicable to all *TORNADO-P6x* DSP systems.

'*TORNADO-P62xx*' notation denotes that the supplied information is applicable to all *TORNADO-P62, TORNADO-P6202* and *TORNADO-P6203* DSP systems.

'*TORNADO-P62xx/P67*' notation denotes that the supplied information is applicable to all *TORNADO-P62, TORNADO-P6202*, *TORNADO-P6203* and *TORNADO-P67* DSP systems.

'*TORNADO-P64xx*' notation denotes that the supplied information is applicable to all *TORNADO-P6414, TORNADO-P6415*, and *TORNADO-P6416* DSP systems.

Should information be a product specific, then the name of the corresponding product (*TORNADO-P62*, *TORNADO-P67, TORNADO-P6202*, *TORNADO-P6203* *TORNADO-P6414*, *TORNADO-P6415*, *TORNADO-P6416*) will be highlighted.

1.1 General Information

TORNADO-P6x are ultra-high performance fixed- and floating-point DSP systems for host PCI-bus computers, and are designed for PCI-bus hosted applications as well as for stand-alone applications. *TORNADO-P6x* DSP systems feature compatible flexible modular system design with optional plug-in daughter-card modules (DCM) in order to meet requirements for virtually any applications while keeping a cost to a minimum.

TORNADO-P6x DSP systems appear as three different boards (fig.1-1):

- *TORNADO-P62* and *TORNADO-P67* DSP systems have been designed using 1st common board (fig.1-1a) with either 200 MHz 32-bit fixed-point TMS320C6201 DSP or 167 MHz 32-bit floating-point TMS320C6701 DSP installed correspondingly
- *TORNADO-P6202* and *TORNADO-P6203* DSP systems have been designed using 2nd common board (fig.1-1b) with either 250 MHz TMS320C6202 or 300 MHz TMS320C6203 32-bit fixed-point DSP installed correspondingly
- *TORNADO-P6414*, *TORNADO-P6415* and *TORNADO-P6416* DSP systems have been designed using 3rd common board (fig.1-1b) with 600 MHz either TMS320C6414, or TMS320C6415, or TMS320C6416 32-bit fixed-point DSP installed correspondingly.

Fig.1-1a. TORNADO-P62/P67 DSP systems board.

Fig.1-1b. TORNADO-P6202/P6203 DSP systems board.

Fig.1-1c. TORNADO-P6414/P6415/P6416 DSP systems board.

CAUTION

TORNADO-P62 and *TORNADO-P67* DSP systems feature identical host PCI interface and on-board DSP environment with the only differences being implied to the DSP performance value and absence/presence of DSP on-chip floating-point unit for TMS320C6201 and TMS320C6701 DSP.

TORNADO-P6202 and *TORNADO-P6203* DSP systems feature identical host PCI interface and on-board DSP environment with the only differences being implied to the DSP performance value and amount of DSP on-chip memory for TMS320C6202 and TMS320C6203 DSP.

All *TORNADO-P6x* DSP systems feature software/hardware compatible host PCI environment and on-board DSP environment, except for the minor differences, which imply to the number of DSP on-chip McBSP ports and programming of the DSP on-chip HPI port.

The following are some applications for *TORNADO-P6x* DSP systems:

- *high-speed multichannel fax/modems*
- *multichannel vocoders and speech signal processing*
- *audio and acoustics signal processing*
- *multimedia*
- *radars, sonars*
- *digital radio*
- *instrumentation and industrial*
- *image processing*
- *TMS320C6x DSP evaluation and education*
- many more ...

TORNADO-P6x utilize TMS320C6x 32-bit fixed- or floating- point DSP (1600 MIPS TMS320C6201 DSP, or 1000 MFLOPS TMS320C6701 DSP, or 2000 MIPS TMS320C6202 DSP, or 2400 MIPS TMS320C6203, or 4800 MIPS TMS320C6414/C6415/C6416 DSP) and feature up to 1 Mbyte on-board dual-port static RAM (DPRAM) for program and data and communication between host PCI-bus and DSP, up to 4 Mbyte on-board synchronous burst static RAM (SBSRAM) for program and data, up to 128 Mbyte on-board synchronous dynamic RAM (SDRAM) for program and data, and up to 1Mx8 EPROM/FLASH for non-volatile data and boot code.

TORNADO-P6x feature high-performance host PCI-bus interface, which offers multi-channel bi-directional communication between host PCI-bus and on-board DSP environment via DPRAM, mailboxes, FIFO and interrupts. DSP can also access host PCI-bus memory and I/O address space using PCI-bus mastering feature. Host PCI-bus interface of *TORNADO-P6x* DSP systems supports data transfers at up to 133 Mbyte/s speed.

TORNADO-P6x offer access to HPI (host port interface) of on-board TMS320C6x DSP from host PCI-bus I/O interface. Along with on-board DPRAM this provides a second data path for communication between host and DSP environment and allows fast access to entire DSP environment including DSP on-chip memory and peripheral registers from host PCI-bus.

TORNADO-P6x feature on-board expansion facilities for installation of serial I/O expansion (SIOX) daughter card modules (DCM). A variety of SIOX DCM includes AD/DA and digital I/O DCM for real-time

instrumentation, industrial and speech, telecommunication and audio signal processing applications. Both SIOX rev.B and SIOX rev.C DCM sites are available.

TORNADO-P6x feature on-board expansion facility for installation of parallel I/O expansion (PIOX/PIOX-16) daughter card module (DCM). A variety of PIOX/PIOX-16 DCM include AD/DA, digital I/O and application specific coprocessor DCM for high-speed real-time instrumentation, industrial and speech, telecommunication and audio signal processing applications. *TORNADO-P6x* provides universal on-board PIOX/PIOX-16 DCM site.

TORNADO-P64xx DSP systems feature on-board UTOPIA level 2 slave interface and general purpose I/O for communication with external industry standard telecommunication UTOPIA master controllers and for interfacing to external 'bit wide' peripherals.

TORNADO-P6x feature optional stand-alone operation, which does not require PCI-bus hosting and allows to boot on-board DSP from on-board FLASH/EPROM after external power has been applied and DSP reset has been released. This is a key point for many DSP applications, which require both PC hosted and stand-alone operation, as well as this allows easy migration from PC hosted DSP software development process to actual stand-alone DSP application with optional SIOX/PIOX AD/DA DCM installed.

TORNADO-P6x use scan-path emulation control for the on-board TMS320C6x DSP in order to debug resident TMS320C6x DSP software. Scan-path emulation control of the on-board TMS320C6x DSP is available either via external TI XDS or MicroLAB' *MIRAGE* JTAG emulators, or by means of *TORNADO-P6x* on-board *emulation controller chip (ECC)*, which comes standard with all *TORNADO-P6x* DSP systems. *ECC* is a low cost identical replacement for TI XDS and MicroLAB Systems *MIRAGE* JTAG emulators and runs under industry standard TI C6000 Code Composer Studio IDE.

TORNADO-P6x DSP software development can be performed using TI TMS320C6000 DSP C/C++ and Assembly compiler tools.

TORNADO-P6x host PC software development can be performed using *TORNADO Software Development Kit* (*TSDK*) for Windows 9x/NT/2000/XP, which provides universal host API for all PC plug-in *TORNADO* DSP systems and can be used with any host PC C/C++ software development tools for Windows. Host DOS utilities and software function libraries are also provided.

TORNADO-P6x are supported by a variety of industry standard 3rd party DSP software tools, which include visual DSP algorithm development tools, real-time operating systems (RTOS), digital filter design tools, DSP/vector/math function libraries, vocoder/fax/modem function libraries, and many more...

1.2 Host PC Specifications

TORNADO-P6x require that host PC must provide at least 80486SX CPU and at least one 33 MHz 32-bit PCI-bus slot.

In order to learn configuration requirements for host PC running TMS320C6x DSP software development and debugging tools, refer to the corresponding original documentation from TI.

1.3 Technical Specification

The following are the technical specifications for *TORNADO-P6x* system.

Parameter description	*parameter value*
power supply voltage	+5V for *TORNADO-P6x* board, optional ±12V for SIOX/PIOX DCM
power consumption	+5V@1.8A (t=+20°C)
on-board DSP	200MHz 1600 MIPS TMS320C6201 (*TORNADO-P62*) 167MHz 1000 MFLOPS TMS320C6701 (*TORNADO-P67*) 250MHz 2000 MIPS TMS320C6202 (*TORNADO-P6202*) 300MHz 2400 MIPS TMS320C6203 (*TORNADO-P6203*) 600MHz 4800 MIPS TMS320C6414 (*TORNADO-P6414*) 600MHz 4800 MIPS TMS320C6415 (*TORNADO-P6415*) 600MHz 4800 MIPS TMS320C6416 (*TORNADO-P6416*)
Dimensions	174x106 mm (6.8"x4.2") fits PCI mini-board size
operating temperature	0..+60°C
I/O expansion interfaces	One site (SIOX-A) for SIOX rev.B DCM, two sites (SIOX-A and SIOX-B) for SIOX rev.C DCM, one site for PIOX/PIOX-16 DCM.
host PCI-bus interface:	
number of active PCI-bus interface areas	4
host PCI-bus requirement	33 MHz 32-bit PCI-bus rev.2 or later
DPRAM capacity	32K/64Kx32 (*TORNADO-P62xx/P67*) 128K/256Kx32 (*TORNADO-P64xx*)
dual-port hardware semaphores (DPSEM) (*TORNADO-P62xx/P67*)	8
size of PCI-bus memory page in the for access to DPRAM via host PCI-bus	8Kx32 (*TORNADO-P62xx/P67*) 128K/256Kx32 (*TORNADO-P62xx/P67*)
host hardware timeout control time for DRRAM ready (*TORNADO-P62xx/P67*), *ECC* ready and HPI ready conditions	2 us
host IRQ lines	INTA, assigned by PCI BIOS
on-board DSP memory:	
SBSRAM	0K/128K/512K/1Mx32 (*TORNADO-P62xx/P67*) 0K/128K/256K/512Kx64 (*TORNADO-P64xx*)

SBSRAM wait states	*TORNADO-P62/P67* : 0ws/1ws depending upon the SBSRAM chips installed (contact MicroLAB Systems for more details) *TORNADO-P6202/P6203* : 1ws *TORNADO-P64xx* : 6ws
SDRAM	0M/4Mx32 1ws (*TORNADO-P62/P67*:) 0M/4M/8Mx32 1ws (*TORNADO-P6202/P6203*) 0M/4M/16Mx64 6ws (*TORNADO-P64xx*)
EPROM	128K..1Mx8 (Ta=100ns), PLCC-32 IC package
FLASH	128K/512Kx8 (Ta=100ns) 5v-only FLASH memory chip, PLCC-32 IC package on-board FLASH write-protection feature
recommended FLASH memory chips	AMD: Am29F010B-90JC 128Kx8 FLASH Am29F040B-90JC 512Kx8 FLASH

watchdog timer:

latency period	0.6 .. 2.0 sec

external clock generators for DSP on-chip McBSP serial ports:

maximum frequency for external clocks for McBSP TMS320C6x DSP serial ports	100 MHz (*TORNADO-P62*) 80MHz (*TORNADO-P67*) 125 MHz (*TORNADO-P6202*) 150 MHz (*TORNADO-P6203*) 300 MHz (*TORNADO-P64xx*)

Chapter 2. System Architecture and Construction

This chapter contains detail description for system architecture and construction of *TORNADO-P6x* DSP systems.

2.1 *TORNADO-P6x* System Architecture

TORNADO-P6x DSP system mainboards install into 32-bit PCI-bus slot of host PC and feature compatible on-board system architectures, which only differ in minor details thus delivering software and hardware compatibility for all for different *TORNADO-P6x* DSP systems. System architectures for different *TORNADO-P6x* DSP systems are presented at figures 2-1a and 2-1b.

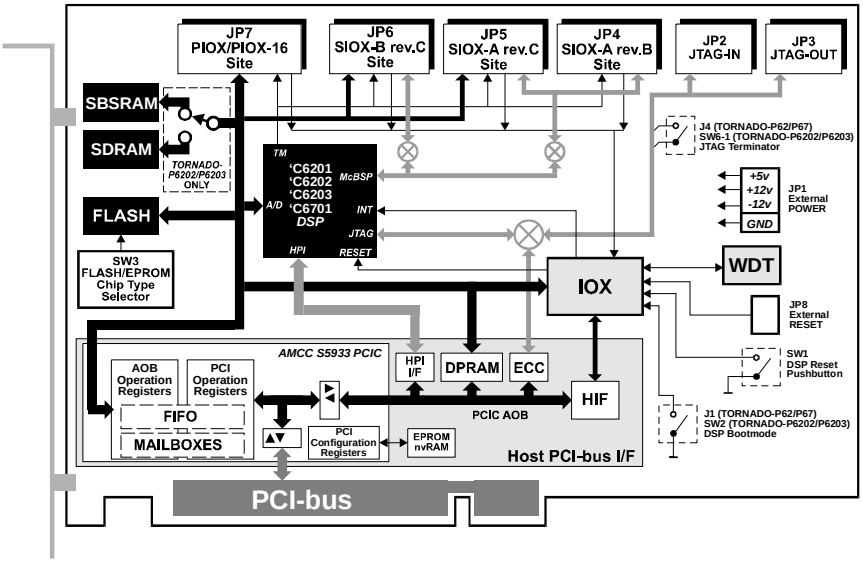


Fig.2-1a. Architecture of *TORNADO-P62xx/P67* DSP systems.

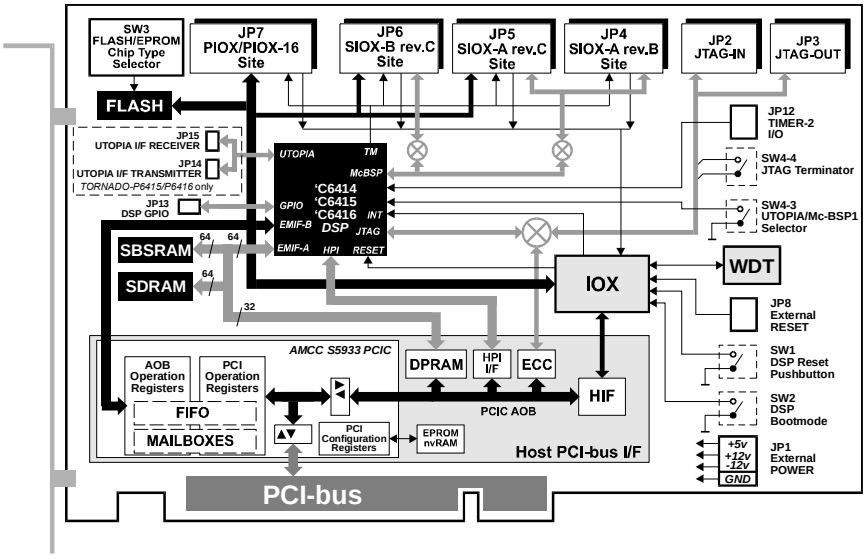


Fig.2-1b. Architecture of *TORNADO-P64xx* DSP systems.

The following is a list of main on-board components for *TORNADO-P6x* DSP systems:

- *32-bit fixed-point TMS320C6201* DSP *(TORNADO-P62)*, or *32-bit floating-point TMS320C6701* DSP *(TORNADO-P67)*, or *32-bit fixed-point TMS320C6202* DSP *(TORNADO-P6202)*, or *32-bit fixed-point TMS320C6203* DSP *(TORNADO-P6203)*, or *32-bit fixed-point TMS320C6414* DSP *(TORNADO-P6414)*, or *32-bit fixed-point TMS320C6415* DSP *(TORNADO-P6415)*, or *32-bit fixed-point TMS320C6416* DSP *(TORNADO-P6416)*
- *synchronous burst RAM (SBSRAM)* for DSP program/data
- *synchronous dynamic RAM (SDRAM)* for DSP program/data
- *dual-port RAM (DPRAM)* for DSP program/data and communication between DSP and host PCI-bus interface
- *socket for FLASH/EPROM* memory chip for DSP source boot code during stand-alone operation
- *DSP I/O expansion controller (IOX)*
- *DSP serial I/O expansion interface (SIOX) sites*, which comprise of SIOX-A rev.B site and SIOX-A/B rev.C sites, for compatible DCM
- *32/16-bit parallel I/O expansion interface (PIOX/PIOX-16) site* for compatible DCM
- *UTOPIA Level 2 slave interface (TORNADO-P6415/P6416)* for communication with external mater telecom controllers
- *10-bit general purpose I/O (TORNADO-P64xx)* for interfacing to external 'bit-wide' peripherals
- *watchdog timer (WDT) and DSP reset switch* for stand-alone operation
- *host PCI-bus interface* with PCI-bus mastering feature
- *emulation controller chip (ECC).*

TORNADO-P6x DSP system has been designed to combine the most powerful and state of the art TI TMS320C6x DSP with high-performance PCI-bus host PC interface. This delivers high-speed communication between host PCI-bus and TMS320C6x DSP environment, and provides outstanding flexibility for I/O

expansion, which has become standard for all *TORNADO* DSP systems and stand-alone controllers. The following are only few main beneficial features of *TORNADO-P6x* DSP systems:

- high-capacity on-board DSP memory pool for program/data
- I/O expansion via a variety of off-the-shelf optional daughter-card modules
- high-performance host PCI-bus providing up to 133 Mbyte/s data transfer speed
- multi-path communication between host PCI-bus and on-board DSP environment via on-board high-density DPRAM without arbitration delays, via TMS320C6x DSP on-chip HPI port, via bi-directional FIFO, via multi-channel bi-directional mailboxes and via multi-source interrupts
- access from on-board DSP to all host PCI-bus memory and I/O areas using PCI-bus mastering feature
- stand-alone operation with watchdog timer and power monitor facilities
- debugging of on-board DSP software via on-board JTAG emulator and industry standard TI C6000 Code Composer Studio IDE.

Construction for different *TORNADO-P6x* boards with specification of all on-board connectors and I/O expansion DCM sites are presented at figures 2-2a, 2-2-b and 2-2c.

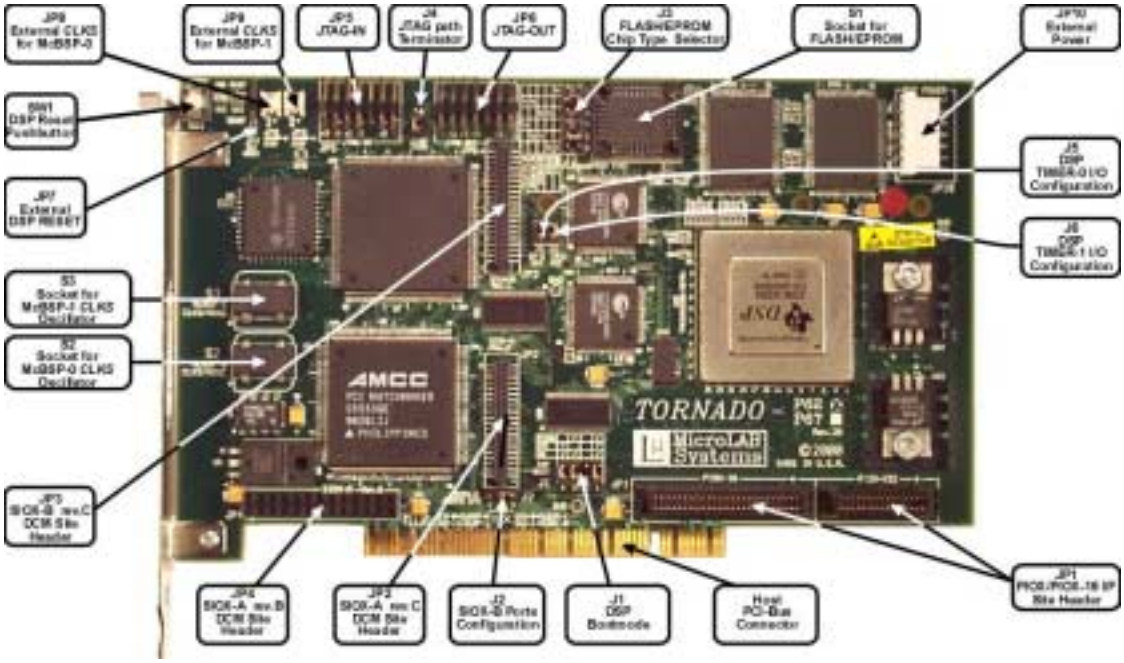


Fig.2-2a. Construction of *TORNADO-P62/P67* board.

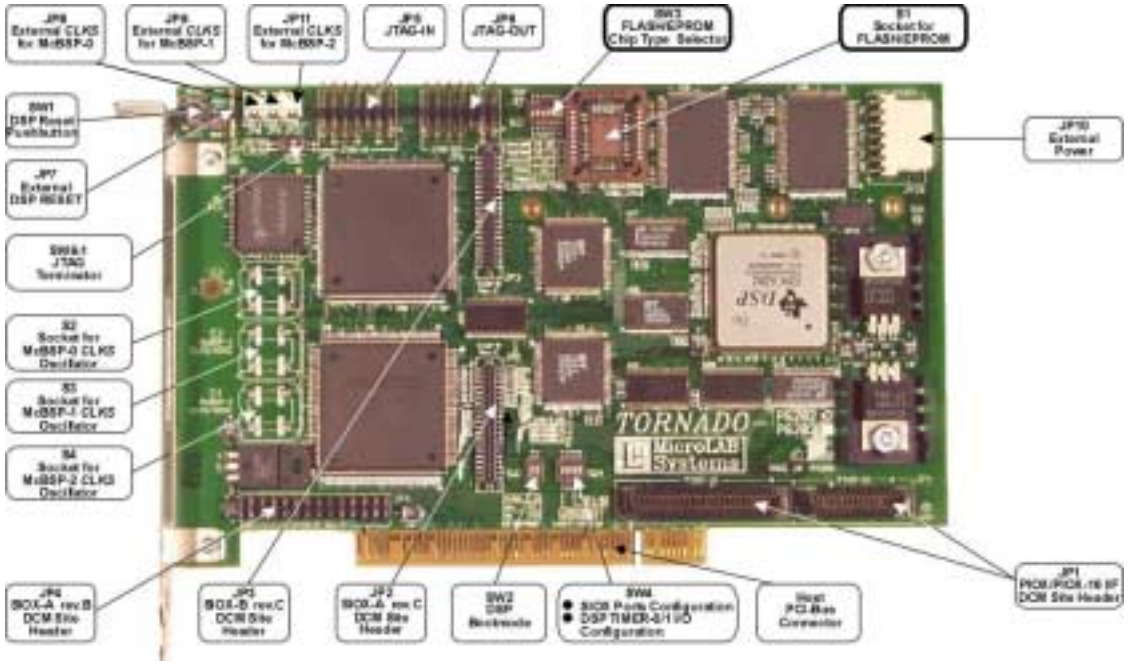


Fig.2-2b. Construction of *TORNADO-P6202/P6203* board.

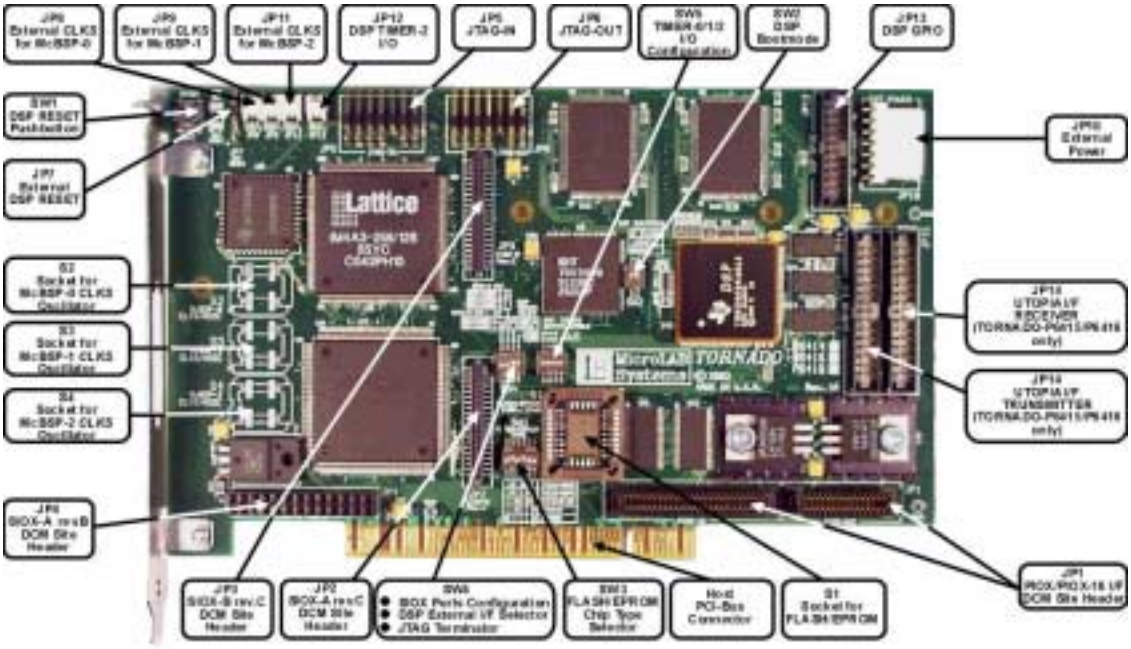


Fig.2-2c. Construction of *TORNADO-P6414/P6415/P6416* board.

TMS320C6x DSP

TORNADO-P6x on-board DSP is defined by particular board name and is one of the code and architecture compatible TI TMS320C6x DSP with VelociTI very-long instruction word (VLIW) on-chip architecture:

- 1600 MIPS @ 200 MHz 32-bit fixed-point TMS320C6201 DSP *(TORNADO-P62)*
- 1000 MFLOPS @ 167 MHz 32-bit floating-point TMS320C6701 DSP *(TORNADO-P67)*
- 2000 MIPS @ 240 MHz 32-bit fixed-point TMS320C6202 DSP *(TORNADO-P6202)*
- 2400 MIPS @ 300 MHz 32-bit fixed-point TMS320C6203 DSP *(TORNADO-P6203)*
- 4800 MIPS @ 600 MHz 32-bit fixed-point TMS320C6414 DSP *(TORNADO-P6414)*
- 4800 MIPS @ 600 MHz 32-bit fixed-point TMS320C6415 DSP *(TORNADO-P6415)*
- 4800 MIPS @ 600 MHz 32-bit fixed-point TMS320C6416 DSP *(TORNADO-P6416)*.

Synchronous Burst Static RAM (SBSRAM)

TORNADO-P62xx/P67 DSP systems provide up to 1Mx32 on-board synchronous burst static RAM (SBSRAM) for TMS320C620x/C6701 DSP program and data, which is mapped to DSP CE-2 EMIF area.

TORNADO-P62/P67 DSP systems allow simultaneous support of on-board SBSRAM and SDRAM by EMIF of on-board TMS320C6201/TMS320C6701 DSP. Number of wait states for DSP-to-SBSRAM access cycles depends upon the speed grades of on-board DSP and SBSRAM chips, and can be set either 0ws or 1ws (contact MicroLAB Systems for SBSRAM wait state details for your *TORNADO-P62/P67* DSP system).

TORNADO-P6202/P6203 DSP systems do not allow simultaneous support of on-board SBSRAM and SDRAM by EMIF of on-board TMS320C6202/TMS320C6203 DSP. Particular currently active external synchronous memory (either SBSRAM or SDRAM) can be selected by DSP software. *TORNADO-P6202/P6203* DSP systems always provide 1 ws for DSP-to-SBSRAM access cycles.

TORNADO-P64xx DSP systems provide up to 512Kx64 on-board SBSRAM for TMS320C64xx DSP program and data, which is mapped to DSP EMIF-A CE-0 area. External 64-bit EMIF-A data bus of *TORNADO-P64xx* on-board TMS320C64xx DSP comprises on-board SBSRAM, SDRAM and DPRAM synchronous memories only in order to minimize DSP delays to external synchronous memory access.

Synchronous Dynamic RAM (SDRAM)

TORNADO-P62/P67 DSP systems provide up to 4Mx32 1ws of on-board synchronous dynamic RAM (SDRAM) for TMS320C6x DSP program and data, which is mapped to DSP CE-3 EMIF area. On-board SBSRAM and SDRAM can be simultaneously supported by EMIF of on-board TMS320C6201/TMS320C6701 DSP of *TORNADO-P62/P67* DSP systems.

TORNADO-P6202/P6203 DSP systems provide up to 8Mx32 1ws of on-board synchronous dynamic RAM (SDRAM) for TMS320C6x DSP program and data, which is mapped to DSP CE-3 and CE-2 EMIF areas. On-board SBSRAM and SDRAM cannot be simultaneously supported by EMIF of on-board TMS320C6202/TMS320C6203 DSP of *TORNADO-P62/P67* DSP systems. Particular currently active external synchronous memory (either SBSRAM or SDRAM) can be selected by DSP software.

TORNADO-P64xx DSP systems provide either 4Mx64 or 128Kx64 on-board SDRAM for TMS320C64xx DSP program and data, which is mapped to DSP EMIF-A CE-3 area. External 64-bit EMIF-A data bus of *TORNADO-P64xx* on-board TMS320C64xx DSP comprises on-board SBSRAM, SDRAM and DPRAM synchronous memories only in order to minimize DSP delays to external synchronous memory access.

FLASH memory

TORNADO-P6x provides up to 1Mx8 on-board FLASH memory bank for DSP boot code during stand-alone operation and for non-volatile data. FLASH memory bank can accommodate both FLASH and EPROM memory chip in PLCC-32 IC package and features write protection circuit for data safety.

For *TORNADO-P62xx/P67* DSP systems, on-board FLASH memory bank is allocated to CE-1 area of TMS320C620x/C6701 DSP EMIF.

For *TORNADO-P64xx* DSP systems, on-board FLASH memory bank is allocated to CE-1 area of TMS320C64xx DSP EMIF-B 16-bit data bus, which comprises all on-board asynchronous peripherals.

Dual-port RAM (DPRAM)

TORNADO-P6x provides on-board dual-port static RAM (DPRAM), which is mapped both to the DSP environment and host PCI-bus memory area.

DPRAM can be used as TMS320C6x DSP external general purpose program and data memory as well as for communication between host PCI-bus and DSP without arbitration delays. Despite to DSP on-chip HPI port, DPRAM allows data upload/download from host PCI-bus while DSP is in the reset state. DPRAM is mapped to the lowest addresses of CE-0 area of DSP' EMIF in order to allow DSP to start program execution from the DPRAM. DPRAM also features built-in mutual interrupt generation (door-bell registers) and eight hardware semaphores.

TORNADO-P62xx/P67 DSP systems provide either 32Kx32 or 64Kx32 on-board asynchronous static DPRAM, which is mapped to TMS320C620x/C6701 DSP CE-0 area and is allocated at DSP 00000000H base address, so DSP can start program execution from DPRAM after DSP reset will be released. *TORNADO-P62xx/P67* on-board DPRAM also provides eight dual-port hardware semaphores, which are useful for synchronization of DSP and host accesses to application specific critical shared memory data allocated in DPRAM.

TORNADO-P64xx DSP systems provide either 128Kx32 or 256Kx32 on-board synchronous static DPRAM, which is mapped to TMS320C64xx DSP EMIF-A CE-1 area. External 64-bit EMIF-A data bus of *TORNADO-P64xx* on-board TMS320C64xx DSP comprises on-board SBSRAM, SDRAM and DPRAM synchronous memories only in order to minimize DSP delays to external synchronous memory access. *TORNADO-P64xx* on-board DPRAM is not allocated at DSP 00000000H base address, so DSP cannot start program execution from DPRAM after DSP reset will be released. *TORNADO-P64xx* on-board DPRAM supports 'PCI burst transfers' at top 133 Mbyte/s speed without wait states to/from host PCI-bus interface.

Host PCI-bus interface

TORNADO-P6x host PCI-bus interface has been designed for DSP and system control, high-speed data transfer between host PCI-bus and on-board DSP environment via FIFO, mailboxes, DPRAM and DSP HPI port, and for emulation control of on-board TMS320C6x DSP via emulation controller chip (ECC) and DSP-on-chip JTAG port.

TORNADO-P6x host PCI-bus interface is based around the AMCC S5933/S5935 Matchmaker PCI controller chip (*PCIC*) and on-board FPGA, and comprises of the following PCI-bus areas:

- *AMCC S5933 PCIC on-chip PCI operation registers*
- *DPRAM area*
- *host interface (HIF) registers and DSP HPI port area*

- *on-board emulator interface (ECC) area*.

CAUTION

TORNADO-P6x DSP systems have been designed to accommodate either AMCC S5933 or compatible S5935 Matchmaker PCI controller (PCIC).

Hereafter, all further reference information provided for AMCC S5933 PCIC is valid for AMCC S5935 PCIC.

Mutual interrupt generation between PCI-bus and DSP is performed via PCIC operation registers and HIF registers. *TORNADO-P6x* DSP system can generate one multi-source maskable interrupt to host PCI-bus and up to four multi-source maskable interrupts to the DSP.

Base addresses for all PCI-bus memory and I/O areas, which are occupied by *TORNADO-P6x* DSP system, are automatically assigned by host PCI BIOS during PC boot procedure.

TMS320C6x HPI (host port interface)

Along with *TORNADO-P6x* on-board DPRAM, host PCI-bus interface delivers access to TMS320C6x on-chip HPI, which comes as a second data path for communication between host PCI-bus and on-board DSP.

Despite DPRAM, HPI offers access from host PCI-bus to all TMS320C6x memory areas (both DSP on-chip and off-chip resources) and allows generation of mutual interrupts between DSP and host PCI-bus. However, unlike DPRAM, HPI does not support random access to DSP memory areas from host PCI-bus, and assumes that the DSP memory address must be pre-latched into HPI address register prior actual HPI data access will be performed. HPI also provides address post-increment feature, which simplifies data array upload/download from host PCI-bus to DSP address areas. HPI is available only while TMS320C6x DSP is executing the program and is not in the reset state.

DSP I/O Expansion Controller (IOX)

TORNADO-P6x has on-board DSP I/O expansion controller (IOX), which provides some extra I/O ports used both locally by the on-board TMS320C6x DSP environment and for communication with host PCI-bus. These extra I/O ports include DSP-to-PCI interrupt request generator, PCI-to-DSP interrupt request generators, DSP external interrupts and non-maskable interrupt selector registers, PCIC FIFO flags status registers, PCI-bus mastering control registers, PIOX/SIOX sites reset control register, watch-dog timer control registers, and more. The IOX area can be accessed by the TMS320C6x DSP only.

Serial I/O Expansion Interface (SIOX) sites

TORNADO-P6x on-board SIOX DCM sites are used for installation of speech/fax/modem AD/DA, telecom interfaces, audio AD/DA, DAT interface, multichannel instrumentation AD/DA/DIO DCM, application specific I/O coprocessor DCM, and many more DCM. This allows immediate ‘off-the-shelf’ re-configuration of *TORNADO-P6x* board in order to meet particular requirements of customer applications for external AD/DA.

On-board SIOX sites suite comprises of one SIOX-A rev.B site, and two SIOX-A/B rev.C sites. SIOX rev.B site comprises of signals for TMS320C6x DSP on-chip McBSP serial ports, timers and interrupt control, whereas SIOX rev.C sites also add 8-bit parallel data bus with 6-bit address and data strobes.

Parallel I/O Expansion Interface (PIOX/PIOX-16) site

TORNADO-P6x feature one universal PIOX/PIOX-16 site for installation of compatible high-speed AD/DA/DIO DCM, multichannel instrumentation AD/DA/DIO DCM, application specific I/O coprocessor DCM, DSP coprocessor DCM, and many more off-the-shelf DCM. This allows immediate 'off-the-shelf' re-configuration of *TORNADO-P6x* board in order to meet particular requirements of customer applications for external AD/DA.

PIOX/PIOX-16 interface comprise of DSP 32-bit data bus, 20-bit address bus, data strobes, and TMS320C6x DSP on-chip timers and interrupt control.

UTOPIA interface (TORNADOPE6415/P6416 only)

TORNADO-P6415/P6416 DSP systems provide on-board 50MHz 8-bit UTOPIA level 2 slave interface for communication with external telecom equipment. UTOPIA interface is part of on-board TMS320C6415/C6416 DSP and is controlled directly by DSP on-chip UTOPIA control registers.

DSP on-chip general purpose digital I/O (TORNADO-P64xx only)

TORNADO-P64xx DSP systems provide optional general purpose 10-bit digital I/O, which is controlled directly by TMS320C64xx DSP on-chip GPIO control registers.

Stand-alone operation

On-board TMS320C6x DSP of *TORNADO-P6x* DSP system can also operate in stand-alone operation mode without host PCI-bus control of DSP reset input.

Stand-alone DSP operation mode is available when *TORNADO-P6x* is installed into host PCI-bus and when *TORNADO-P6x* board is unplugged from host PCI-bus slot and operates as stand-alone DSP controller in embedded DSP applications with external power applied via on-board dedicated power connector. In case *TORNADO-P6x* board is unplugged from host PCI-bus slot, then on-board AMCC PCIC is not available for access from on-board DSP and PCI-bus is not available.

Stand-alone DSP operation mode of *TORNADO-P6x* DSP systems allows easy migration from target system software debugging using host PC to real-time embedded DSP application.

Stand-alone DSP operation mode can be set by host PC software via HIF registers in case *TORNADO-P6x* is installed into host PCI-bus slot, and is selected automatically in case *TORNADO-P6x* board is unplugged from host PCI-bus slot.

During stand-alone DSP operation mode, the DSP source program/data can bootload either from on-board FLASH/EPROM memory, or HPI port of TMS320C6x DSP (in case *TORNADO-P6x* board is installed into host PCI-bus slot) after the DSP reset line has been released. The particular boot mode is defined by on-board DSP bootmode jumpers/switches. The on-board FLASH memory can be programmed either via host PCI-bus interface while *TORNADO-P6x* is installed into host PC, or can be programmed anytime directly by on-board

DSP. TMS320C6x DSP on-chip HPI port is available via host PCI-bus interface only when *TORNADO-P6x* board is installed into host PCI-bus slot.

Watchdog Timer (WDT)

TORNADO-P6x features the on-board watchdog timer (WDT), which might be used during stand-alone DSP reset mode in order to increase system reliability. In case WDT is enabled by the DSP software, then DSP software must periodically reset WDT with the period about 0.8 sec, otherwise WDT will provide automatic DSP reset and restart of DSP program (in case DSP software either hangs-on or idles for more than 0.8 sec).

DSP external interrupts and NMI

TORNADO-P6x features multi-source DSP software configured four DSP external interrupts and NMI. The interrupt sources comprise of output PCIC interrupt, FIFO read/write interrupts, external SIOX/PIOX interrupts, DPRAM interrupt, and two host-to-DSP interrupts in order to meet requirements of many applications. Selection of particular interrupt source for each of four DSP external interrupts and NMI is performed by means of the corresponding interrupt selector registers, which are the part of the DSP IOX controller.

Debugging of resident TMS320C6x DSP software

TMS320C6x DSP software for *TORNADO-P6x* DSP systems can be debugged via TI C6000 Code Composer Studio debugger either with external TI XDS and MicroLAB' *MIRAGE* JTAG emulators, or via *TORNADO-P6x* on-board emulation controller chip (*ECC*). *TORNADO-P6x* on-board *ECC* is direct replacement for external JTAG emulators. However, in case *TORNADO-P6x* application requires intensive communication between host PCI-bus and on-board DSP environment, it is recommended to use external JTAG emulator in order to get higher flexibility and to provide host PC software safety and integrity during DSP software development.

Key differences between TORNADO-P62xx/P67 and TORNADO-P64xx DSP systems

It is important to highlight principal architecture differences between *TORNADO-P62xx/P67* (fig.2-1a) and *TORNADO-P64xx* DSP systems (fig.2-1b).

TORNADO-P64xx DSP systems have been designed using TI TMS320C64xx DSP, which feature external dual-bus (EMIF) DSP architecture, and therefore, all *TORNADO-P64xx* DSP systems have been designed to benefit from this in order to principally increase data transfer performance inside DSP and host PCI-bus interface environments. Instead, all *TORNADO-P62xx/P67* DSP systems have been designed using TI TMS320C620x/C6701 DSP, which feature external single-bus DSP architecture.

At first, for *TORNADO-P64xx* DSP systems, on-board SBSRAM, SDRAM and DPRAM memories are connected to TMS320C64xx DSP EMIF-A 64-bit data bus, which is isolated from TMS320C64xx DSP EMIF-B 16-bit data bus comprising all on-board asynchronous peripherals (IOX, PCIC, PIOX/PIOX-16 and SIOX-A/B rev.C parallel data buses). Instead, for all *TORNADO-P62xx/P67* DSP systems, all on-board SBSRAM, SDRAM and DPRAM memories and all on-board asynchronous peripherals (IOX, PCIC, PIOX/PIOX-16 and SIOX-A/B rev.C parallel data buses) are connected to single external 32-bit data bus of TMS320C64xx DSP. As a result, *TORNADO-P64xx* DSP systems feature significant increase of DSP external I/O data transfer performance against all *TORNADO-P62xx/P67* DSP systems and allow simultaneous parallel access from on-board DSP to external memories and asynchronous peripherals through different data buses. This is extremely important for DMA transfers between on-board PIOX/PIOX-16 DCM site and DSP memory environment.

At second, for *TORNADO-P64xx* DSP systems, on-board DPRAM is a synchronous memory device instead of asynchronous memory used in *TORNADO-P62xx/P67* DSP systems. This allows to significantly increase DSP-to-DPRAM data transfer performance for *TORNADO-P64xx* DSP systems and to perform PCI-to-DPRAM data transfers at maximum possible 133 Mbyte/s speed using true 'PCI burst transfers' without PCI-bus wait states. 'PCI burst transfers' to/from *TORNADO-P64xx* on-board DPRAM are automatically inserted by PCI-bus controller and handled by on-board hardware in case host PC application initializes bulk data transfers to/from on-board DPRAM.

At third, due to different memory maps for TI TMS320C64xx and TMS320C620x/C6701 DSP, *TORNADO-P64xx* and *TORNADO-P62xx/P67* DSP systems feature different DSP memory maps (refer to tables 2-1a and 2-1b for more details).

At fourth, *TORNADO-P64xx* DSP systems provide UTOPIA level 2 slave interface (*TORNADO-P6415/P6416*) and 10-bit general purpose I/O as standard TMS320C64xx DSP on-chip peripherals, which are not available at TMS320C620x/C6701 DSP.

At fifth, the minor difference between *TORNADO-P64xx* and *TORNADO-P62xx/P67* DSP systems is that *TORNADO-P64xx* allows to set DSP bootmode from host PC software when the board is installed into host PCI-bus slot, which is very beneficial for many host PC applications. Instead, *TORNADO-P62xx/P67* DSP systems allow to set DSP bootmode only via on-board jumpers/switches.

2.2 TMS320C6x DSP Environment

The *TORNADO-P6x* DSP systems utilize state of art TMS320C6x ultra-high performance code compatible 32-bit fixed- and floating point DSP from TI:

- 1600 MIPS 32-bit fixed-point TMS320C6201 DSP in *TORNADO-P62* DSP system
- 1000 MFLOPS 32-bit floating-point TMS320C6701 DSP in *TORNADO-P67* DSP system
- 2000 MIPS 32-bit fixed-point TMS320C6202 DSP in *TORNADO-P6202* DSP system
- 2400 MIPS @ 300 MHz 32-bit fixed-point TMS320C6203 DSP in *TORNADO-P6203* DSP system
- 4800 MIPS @ 600 MHz 32-bit fixed-point TMS320C6414 DSP in *TORNADO-P6414* DSP system
- 4800 MIPS @ 600 MHz 32-bit fixed-point TMS320C6415 DSP in *TORNADO-P6415* DSP system
- 4800 MIPS @ 600 MHz 32-bit fixed-point TMS320C6416 DSP in *TORNADO-P6416* DSP system.

All TMS320C6x DSP feature code compatibility (except for different memory maps for *TORNADO-P64xx* and *TORNADO-P62xx/P67* DSP systems), compatible DSP environment, compatible architecture, and compatible peripherals. The only differences apply to capacity of DSP on-chip RAM, number of DSP on-chip McBSP ports, DSP on-chip HPI port, DSP on-chip UTOPIA interface and DSP on-chip general purpose I/O.

CAUTION

This manual does not contain description and programming details for TI TMS320C6x DSP.

For more information about TMS320C6x DSP refer to original TI datasheets and user's guides, which are supplied in either paper or electronic form along with this manual.

TMS32C6x DSP Endian Mde

TORNADO-P6x DSP systems have been designed for little endian mode of on-board TMS320C6x DSP only. Big endian mode of on-board TMS320C6x DSP is not supported.

TMS320C6x DSP memory map

Due to the different memory maps for external memories and I/O peripherals for TMS320C62xx/C6701 and TMS320C64xx DSP, DSP memory maps for *TORNADO-P62xx/P67* on-board TMS320C62xx/C6701 DSP and for *TORNADO-P64xx* on-board TMS320C64xx DSP are not compatible.

CAUTION

TMS320C62xx/C6701 DSP applications, which are compiled for *TORNADO-P62xx/P67* DSP systems and which use onboard SBSRAM, SDRAM, DPRAM, FLASH, external peripherals and control registers, will not run at *TORNADO-P64xx* DSP systems.

Vice-versa, TMS320C64xx DSP applications, which are compiled for *TORNADO-P64xx* DSP systems and which use onboard SBSRAM, SDRAM, DPRAM, FLASH, external peripherals and control registers, will not run at *TORNADO-P62xx/P67* DSP systems.

Memory maps for on-board TMS320C6x DSP for different *TORNADO-P6x* DSP systems are presented in tables 2-1a and 2-1b.

TORNADO-P62xx/P67 on-board TMS320C620x/C6701 DSP supports four external memory areas (table 2-1a):

- EMIF CE-0 area, which controls on-board DPRAM/DPSEM memory, AMCC S5933 PCIC AOB registers, IOX registers, parallel data port of SIOX rev.C DCM sites, and PIOX/PIOX-16 DCM site
- EMIF CE-1 area, which controls on-board FLASH/EPROM memory
- EMIF CE-2 area, which controls on-board SBSRAM memory for *TORNADO-P62/P67* DSP systems, and shared SBSRAM memory and optional SDRAM-1 memory bank for *TORNADO-P6202/P6203* DSP systems. Selection between SBSRAM and SDRAM memory in EMIF CE-2 area for *TORNADO-P6202/P6203* DSP systems is performed via bit *XMEM* of *DSP_SYS_STAT_RG* IOX register (refer to the corresponding subsection below).
- EMIF CE-3 area, which controls on-board primary SDRAM memory. SDRAM memory bank in EMIF CE-3 area for *TORNADO-P6202/P6203* DSP systems is activated along with optional SDRAM-1 bank via bit *XMEM* of *DSP_SYS_STAT_RG* IOX register (refer to the corresponding subsection below).

TORNADO-P64xx on-board TMS320C64xx DSP supports the following external memory areas (table 2-1b):

- EMIF-A CE-0 area, which controls on-board 64-bit SBSRAM memory bank
- EMIF-A CE-1 area, which controls on-board 32-bit DPRAM memory bank
- EMIF-A CE-2 area, which controls on-board 64-bit SDRAM memory bank
- EMIF-B CE-0 area, which controls on-board AMCC S5933 PCIC AOB registers, IOX registers, and parallel data bus of SIOX rev.C DCM sites
- EMIF-B CE-1 area, which controls on-board FLASH/EPROM memory
- EMIF-B CE-3 area, which controls on-board parallel data bus of PIOX/PIOX-16 DCM site.

CAUTION

TMS320C6x DSP address space for all *TORNADO-P6x* DSP systems is the address space for 8-bit (byte) data words.

16-bit data words are allocated on the x2 address boundaries.

32-bit data words are allocated on x4 address boundaries.

Table 2-1a. Memory map for TMS320C620x/C6701 DSP of *TORNADO-P62xx/P67* DSP systems.

memory area of TMS320C620x/C6701 DSP	DSP address range (in bytes)	valid data bits	value at DSP RESET	Access mode	wait states	EMIF CE area and mode
On-board (DSP off-chip) memories						
DPRAM	00000000H ..0001FFF7H (32Kx32) 00000000H ..0003FFF7H (64Kx32)	D0..D31	-	r/w	AWS +*DP_RDY*	CE-0 ASYNC mode
DPRAM: *DPRAM_HM_RQ* register (PCI-to-DSP interrupt request via DPRAM)	0001FFFCH (32Kx32) 0003FFFCH (64Kx32)	D0..D31	-	r/w	AWS +*DP_RDY*	
DPRAM: *DPRAM_MH_RQ* register (DSP-to-DSP interrupt request via DPRAM)	0001FFF8H (32Kx32) 0003FFF8H (64Kx32)	D0..D31	-	r/w	AWS +*DP_RDY*	
DPSEM (dual-port semaphores)	00080000H ..0008001FH	D0 only	-	r/w	AWS	
FLASH/EPROM	01000000H ..013FFFFFH	D0..D7	-	r/w (with write disable)	FWS	CE-1 ASYNC ROM mode

SBSRAM (*TORNADO-P62/P67*)	02000000H ..023FFFFFH	D0..D31	-	r/w	0/1ws[7)]	CE-2 SBSRAM mode
SBSRAM (*TORNADO-P6202/P6203*)	02000000H ..023FFFFFH				1ws	SBSRAM mode
SDRAM (*TORNADO-P6202/P6203*)	02000000H ..02FFFFFFH				1ws	SDRAM mode
SDRAM	03000000H ..03FFFFFFH	D0..D31	-	r/w	1ws	CE-3 SDRAM mode
AMCC S5933 PCIC and IOX registers						
S5933 PCIC area: *DSP_PCIC_FIFO_RG* register (32-bit data format only) (Read-FIFO and Write-FIFO)	000C0000H	D0..D31	-	r/w @A32	AWS +[3)]	CE-0 ASYNC mode
S5933 PCIC area: *DSP_PCIC_AMBEF_RG* register	000C0004H	D0..D31	-	R	AWS +[3)]	
S5933 PCIC area: *DSP_PCIC_AINT_RG* register	000C0008H	D0..D31	-	r/w	AWS +[3)]	
S5933 PCIC area: *DSP_PCIC_AGCSTS_RG* register	000C000CH	D0..D31	-	r/w	AWS +[3)]	
S5933 PCIC area: *DSP_PCIC_MWAR_RG* register	000C0010H	D0..D31	-	r/w	AWS +[3)]	
S5933 PCIC area: *DSP_PCIC_MWTC_RG* register	000C0014H	D0..D31	-	r/w	AWS +[3)]	
S5933 PCIC area: *DSP_PCIC_MRAR_RG* register	000C0018H	D0..D31	-	r/w	AWS +[3)]	
S5933 PCIC area: *DSP_PCIC_MRTC_RG* register	000C001CH	D0..D31	-	r/w	AWS +[3)]	

S5933 PCIC area: *DSP_PCIC_IMBX0_RG* register (Incoming MBX-1)	000C0020H	D0..D31	-	R	AWS +[3)]
S5933 PCIC area: *DSP_PCIC_IMBX1_RG* register (Incoming MBX-2)	000C0024H	D0..D31	-	R	AWS +[3)]
S5933 PCIC area: *DSP_PCIC_IMBX2_RG* register (Incoming MBX-3)	000C0028H	D0..D31	-	R	AWS +[3)]
S5933 PCIC area: *PCIC_IMBX3_RG* register (Incoming MBX-4)	000C002CH	D0..D31	-	R	AWS +[3)]
S5933 PCIC area: *DSP_PCIC_OMBX0_RG* register (Outgoing MBX-1)	000C0030H	D0..D31	-	r/w	AWS +[3)]
S5933 PCIC area: *DSP_PCIC_OMBX1_RG* register (Outgoing MBX-2)	000C0034H	D0..D31	-	r/w	AWS +[3)]
S5933 PCIC area: *DSP_PCIC_OMBX2_RG* register (Outgoing MBX-3)	000C0038H	D0..D31	-	r/w	AWS +[3)]
S5933 PCIC area: *DSP_PCIC_OMBX3_RG* register (Outgoing MBX-4)	000C003CH	D0..D31	-	r/w	AWS +[3)]
IOX area: *DSP_FIFO_STAT_RG* register (PCIC FIFO status)	000C0040H	D0..D3	-	R	AWS
IOX area: *DSP_AWREN_RG* register (PCI-bus mastering control)	000C0044H	D0..D3	0	r/w	AWS
IOX area: *MH_RQ* register (DSP-to-PCI request)	000C0050H	write data is ignored	-	W	AWS

IOX area: *DSP_PXSX_RESET_RG* register (reset control for PIOX and SIOX DCM sites)	000C0054H	D0..D3	0	r/w	AWS
IOX area: *DSP_SYS_STAT_RG* register (system information)	000C0058H	D0..D3	-	r/w	AWS
IOX area: *DSP_WDT_CLR_RG* register (clear watch-dog timer)	000c005CH	write data is ignored	-	W	100ns (hardware controlled) + AFWS
IOX area: *DSP_DEV_ID_RG* register (device ID for *TORNADO-P6202/P6203* DSP systems)	000c005CH	D0..D3	-	R	AWS
IOX area: *DSP_WDT_EN_RG* register (WDT enable for stand-alone operation)	000c0060H	D0..D3	0	r/w	AWS
IOX area: *DSP_HM_RQ0_RG* register (PCI-to-DSP request #0)	000C0064H	D0..D3 write data is ignored	-	r w	AWS
IOX area: *DSP_HM_RQ1_RG* register (PCI-to-DSP request #1)	000C0068H	D0..D3 write data is ignored	-	R w	AWS
IOX area: *DSP_NMI_SEL_RG* register (DSP NMI source selector)	000C006CH	D0..D3	0H	r/w	AWS
IOX area: *DSP_EXT_INT4_SEL_RG* register (DSP EXT_INT4 source selector)	000C0070H	D0..D3	0H	r/w	AWS
IOX area: *DSP_EXT_INT5_SEL_RG* register (DSP EXT_INT5 source selector)	000C0074H	D0..D3	0H	r/w	AWS

IOX area: *DSP_EXT_INT6_SEL_RG* register (DSP EXT_INT6 source selector)	000C0078H	D0..D3	0H	r/w	AWS	
IOX area: *DSP_EXT_INT7_SEL_RG* register (DSP EXT_INT7source selector)	000C007CH	D0..D3	0H	r/w	AWS	
Parallel data buses of on-board DCM sites						
Parallel data bus of SIOX-A rev.C DCM site interface	00100000H ..0010003FH	D0..D7	-	r/w	AWS +*SXA_RDY*	CE-0 ASYNC mode
Parallel data bus of SIOX-B rev.C DCM site interface	00140000H ..0014003FH	D0..D7	-	r/w	AWS +*SXB_RDY*	
Parallel data bus of PIOX DCM site interface	00200000H ..003FFFFFH	D0..D31	-	r/w	AWS +*PX_RDY*	
Parallel data bus of PIOX-16 DCM site interface	00200000H ..0023FFFFH	D0..D15	-	r/w @A16 @A32	AWS +*PX_RDY*	
DSP on-chip memory and peripheral registers						
DSP on-chip program RAM	01400000H ..0140FFFFH (*TORNADO-P62/P67*) 01400000H ..0143FFFFH (*TORNADO-P6202*) 01400000H ..0145FFFFH (*TORNADO-P6203*)	D0..D31	-	r/w	-	-
DSP on-chip peripheral registers	01800000H ..01FFFFFFH	D0..D31	-	r/w	-	-

DSP on-chip data RAM	80000000H ..8000FFFFH (*TORNADO-P62/P67*) 80000000H ..8001FFFFH (*TORNADO-P6202*) 80000000H ..8007FFFFH (*TORNADO-P6203*)	D0..D31	-	r/w	-	-

Notes:

1. IOX area denotes on-board I/O expansion controller.
2. S5933 PCIC area denotes AMCC S5933 PCI Matchmaker Controller AOB operation registers.
3. Accesses to the AOB registers of S5933 PCI Matchmaker Controller require additional wait states depending upon the type of current host PCI-bus interface operation and eventual synchronization between the PCI-bus clock and the DSP clock.
4. *AWS* denotes number of software programmed wait states for accessing asynchronous EMIF CE-0 area, which is a sum of read/write strobe wait states, read/write setup wait states and read/write hold wait states. Refer to the corresponding subsection below for more details.
5. *AFWS* denotes number of software programmed framing wait states for accessing asynchronous EMIF CE-0 area, which is a sum of read/write setup wait states and read/write hold wait states. Refer to the corresponding subsection below for more details.
6. *DP_RDY*, *SXA_RDY*, *SXB_RDY* and *PX_RDY* denote extra wait states, which can be generated by external hardware ready signals for on-board DPRAM, SIOX-A rev.C site, SIOX-B rev.C site and PIOX/PIOX-16 site. Refer to the corresponding subsection below for more details about DPRAM and the corresponding sections later in this chapter for more details about SIOX and PIOX/PIOX DCM sites.
7. Number of programmed wait states (either 0ws or 1ws) for on-board SBSRAM bank of *TORNADO-P62/P67* DSP systems depends upon the speed grade of particular SBSRAM chips installed. Refer to the corresponding subsection below for more details.
8. Other DSP memory and I/O areas are reserved. Do not use these address areas.
9. Register access modes: *r* - read only, *w* - write only, *r/w* - read/write.
10. If specified in the ‘access mode’ field, @A8 denotes that access can be performed using 8-bit word only, @A16 denotes that access can be performed using 16-bit word only, and @A32 denotes that access can be performed using 32-bit word only. If none of the above is specified in the ‘access mode’ field, then access can be performed using any of 8/16/32-bit words.

Table 2-1b. Memory map for TMS320C64xx DSP of *TORNADO-P64xx* DSP systems.

memory area of TMS320C64xx DSP	DSP address range (in bytes)	valid data bits	value at DSP RESET	Access mode	wait states	EMIF CE area and mode
On-board (DSP off-chip) memories						
SBSRAM	80000000H ..800FFFFFH (128Kx64) 80000000H ..801FFFFFH (256Kx64) 80000000H ..803FFFFFH (512Kx64)	D0..D31	-	r/w	6ws	EMIF-A CE-0 SBSRAM mode
DPRAM	90000000H ..9007FFFFH (128Kx32) 90000000H ..900FFFFFH (256Kx32)	D0..D31	-	r/w	6ws	EMIF-A CE-1 SBSRAM mode
DPRAM: *DPRAM_HM_RQ* register (PCI-to-DSP interrupt request via DPRAM) (256Kx32 DPRAM only)	000FFFFCH (256Kx32)	D0..D31	-	r/w	6ws	
DPRAM: *DPRAM_MH_RQ* register (DSP-to-DSP interrupt request via DPRAM) (256Kx32 DPRAM only)	000FFFF8H (256Kx32)	D0..D31	-	r/w	6ws	
SDRAM	A0000000H ..A1FFFFFFH (4Mx64) A0000000H ..A7FFFFFFH (16Mx64)	D0..D31	-	r/w	1ws	EMIF-A CE-2 SDRAM mode
FLASH/EPROM	64000000H ..641FFFFFH (1Mx8)	D0..D7 @W16	-	r/w @A8 @A16 (with write disable)	FWS	EMIF-B CE-1 ASYNC ROM mode

AMCC S5933 PCIC and IOX registers						
S5933 PCIC area: *DSP_PCIC_FIFO_RG* register (32-bit data format only) (Read-FIFO and Write-FIFO)	60000000H	D0..D31 @W32	-	r/w @A32	AWS +[3)]	CE-0 ASYNC mode
S5933 PCIC area: *DSP_PCIC_AMBEF_RG* register	60000004H	D0..D31 @W32	-	R	AWS +[3)]	
S5933 PCIC area: *DSP_PCIC_AINT_RG* register	60000008H	D0..D31 @W32	-	r/w	AWS +[3)]	
S5933 PCIC area: *DSP_PCIC_AGCSTS_RG* register	6000000CH	D0..D31 @W32	-	r/w	AWS +[3)]	
S5933 PCIC area: *DSP_PCIC_MWAR_RG* register	60000010H	D0..D31 @W32	-	r/w	AWS +[3)]	
S5933 PCIC area: *DSP_PCIC_MWTC_RG* register	60000014H	D0..D31 @W32	-	r/w	AWS +[3)]	
S5933 PCIC area: *DSP_PCIC_MRAR_RG* register	60000018H	D0..D31 @W32	-	r/w	AWS +[3)]	
S5933 PCIC area: *DSP_PCIC_MRTC_RG* register	6000001CH	D0..D31 @W32	-	r/w	AWS +[3)]	
S5933 PCIC area: *DSP_PCIC_IMBX0_RG* register (Incoming MBX-1)	60000020H	D0..D31 @W32	-	R	AWS +[3)]	
S5933 PCIC area: *DSP_PCIC_IMBX1_RG* register (Incoming MBX-2)	60000024H	D0..D31 @W32	-	R	AWS +[3)]	
S5933 PCIC area: *DSP_PCIC_IMBX2_RG* register (Incoming MBX-3)	60000028H	D0..D31 @W32	-	R	AWS +[3)]	
S5933 PCIC area: *PCIC_IMBX3_RG* register (Incoming MBX-4)	6000002CH	D0..D31 @W32	-	R	AWS +[3)]	

S5933 PCIC area: *DSP_PCIC_OMBX0_RG* register (Outgoing MBX-1)	60000030H	D0..D31 @W32	-	r/w	AWS +[3)]
S5933 PCIC area: *DSP_PCIC_OMBX1_RG* register (Outgoing MBX-2)	60000034H	D0..D31 @W32	-	r/w	AWS +[3)]
S5933 PCIC area: *DSP_PCIC_OMBX2_RG* register (Outgoing MBX-3)	60000038H	D0..D31 @W32	-	r/w	AWS +[3)]
S5933 PCIC area: *DSP_PCIC_OMBX3_RG* register (Outgoing MBX-4)	6000003CH	D0..D31 @W32	-	r/w	AWS +[3)]
IOX area: *DSP_FIFO_STAT_RG* register (PCIC FIFO status)	60000040H	D0..D7 @W32	-	R	AWS
IOX area: *DSP_AWREN_RG* register (PCI-bus mastering control)	60000044H	D0..D7 @W32	0	r/w	AWS
IOX area: *DSP_XIO_FMT_RG* register (external I/O format control)	6000004CH	D0..D7 @W32	0	r/w	AWS
IOX area: *MH_RQ* register (DSP-to-PCI request)	60000050H	Write data is ignored @W32	-	W	AWS
IOX area: *DSP_PXSX_RESET_RG* register (reset control for PIOX and SIOX DCM sites)	60000054H	D0..D7 @W32	0	r/w	AWS
IOX area: *DSP_SYS_STAT_RG* register (system information)	60000058H	D0..D7 @W32	-	R	AWS
IOX area: *DSP_WDT_CLR_RG* register (clear watch-dog timer)	6000005CH	Write data is ignored @W32	-	W	100ns (hardware controlled) + AFWS

IOX area: *DSP_DEV_ID_RG* register (device ID)	6000005CH	D0..D7 @W32	-	R	AWS
IOX area: *DSP_WDT_EN_RG* register (WDT enable for stand-alone operation)	60000060H	D0..D7 @W32	0	r/w	AWS
IOX area: *DSP_HM_RQ0_RG* register (PCI-to-DSP request #0)	60000064H	D0..D7 @W32 write data is ignored	-	R w	AWS
IOX area: *DSP_HM_RQ1_RG* register (PCI-to-DSP request #1)	60000068H	D0..D7 @W32 write data is ignored	-	R w	AWS
IOX area: *DSP_NMI_SEL_RG* register (DSP NMI source selector)	6000006CH	D0..D7 @W32	0H	r/w	AWS
IOX area: *DSP_EXT_INT4_SEL_RG* register (DSP EXT_INT4 source selector)	60000070H	D0..D7 @W32	0H	r/w	AWS
IOX area: *DSP_EXT_INT5_SEL_RG* register (DSP EXT_INT5 source selector)	60000074H	D0..D7 @W32	0H	r/w	AWS
IOX area: *DSP_EXT_INT6_SEL_RG* register (DSP EXT_INT6 source selector)	60000078H	D0..D7 @W32	0H	r/w	AWS
IOX area: *DSP_EXT_INT7_SEL_RG* register (DSP EXT_INT7source selector)	6000007CH	D0..D7 @W32	0H	r/w	AWS

Parallel data buses of on-board DCM sites						
Parallel data bus of SIOX-A rev.C DCM site interface	60100000H ..6010007FH	D0..D7 @W32	-	r/w	AWS +*SXA_RDY*	EMIF-B CE-0 ASYNC mode
Parallel data bus of SIOX-B rev.C DCM site interface	60180000H ..6018007FH	D0..D7 @W32	-	r/w	AWS +*SXB_RDY*	
Parallel data bus of PIOX DCM site interface	6C000000H ..6C1FFFFFH	D0..D31 @W32	-	r/w	AWS +*PX_RDY*	EMIF-B CE-3 ASYNC mode
Parallel data bus of PIOX-16 DCM site interface	6C000000H ..6C03FFFFH	D0..D15 @W32	-	r/w @A16 @A32	AWS +*PX_RDY*	
DSP on-chip memory and peripheral registers						
DSP on-chip RAM	00000000H ..000FFFFFH	D0..D31	-	r/w	-	-
DSP on-chip peripheral registers	01800000H ..02000033H	D0..D31	-	r/w	-	-

Notes:

1. IOX area denotes on-board I/O expansion controller.
2. S5933 PCIC area denotes AMCC S5933 PCI Matchmaker Controller AOB operation registers.
3. Accesses to the AOB registers of S5933 PCI Matchmaker Controller require additional wait states depending upon the type of current host PCI-bus interface operation and eventual synchronization between the PCI-bus clock and the DSP clock.
4. *AWS* denotes number of software programmed wait states for accessing corresponding asynchronous EMIF-A/B CE area, which is a sum of read/write strobe wait states, read/write setup wait states and read/write hold wait states. Refer to the corresponding subsection below for more details.
5. *AFWS* denotes number of software programmed framing wait states for accessing asynchronous EMIF CE-0 area, which is a sum of read/write setup wait states and read/write hold wait states. Refer to the corresponding subsection below for more details.
6. *SXA_RDY*, *SXB_RDY* and *PX_RDY* denote extra wait states, which can be generated by external hardware ready signals for on-board SIOX-A rev.C site, SIOX-B rev.C site and PIOX/PIOX-16 DCM sites. Refer to the corresponding subsection below for more details about DPRAM and the corresponding sections later in this chapter for more details about SIOX and PIOX/PIOX-16 DCM sites.
7. @W16 and @W32 denotes that the address step for consecutive data words of this area corresponds to 16-bit and 32-bit data words correspondingly. Refer to the corresponding subsection below for more details.
8. Other DSP memory and I/O areas are reserved. Do not use these address areas.
9. Register access modes: *r* - read only, *w* - write only, *r/w* - read/write.
10. If specified in the 'access mode' field, @A8 denotes that access can be performed using 8-bit word only, @A16 denotes that access can be performed using 16-bit word only, and @A32 denotes that access can be performed using 32-bit word only. If none of the above is specified in the 'access mode' field, then access can be performed using any of 8/16/32-bit words.

TMS320C6x DSP bootmode configurations

TORNADO-P6x DSP systems allow to configure on-board TMS320C6x to start in different DSP bootmodes in order to meet requirements of different applications. *TORNADO-P62xx/P67* DSP systems allow to set DSP bootmode via on-board jumpers/switches only, whereas *TORNADO-P64xx* DSP systems provides more flexibility and allow to set DSP bootmode via host PC software and on-board jumpers/switches.

Bootmode configuration for *TORNADO-P62/P67* on-board DSP can be selected via on-board J1 jumper set, whereas bootmode configuration for *TORNADO-P6202/P6203* on-board DSP can be set via on-board SW2 switch (see fig.2-2 and fig.A-1). Supported DSP bootmode configurations for *TORNADO-P62xx/P67* DSP systems are presented in table 2-2a.

CAUTION

DSP bootmode configuration for *TORNADO-P62xx/P67* DSP systems cannot be set via host PC software.

Table 2-2a. TMS320C620x/C6701 DSP Bootmode Configurations for *TORNADO-P62xx/P67*.

'C620x/C6701 DSP Bootmode	**Description**	***TORNADO-P62/P67* on-board J1 jumper set**				***TORNADO-P6202/P6203* on-board SW2 switch**	
		J1-4	**J1-3**	**J1-2**	**J1-1**	**SW2-1**	**SW2-2**
BM#2 (NO BOOT)	*No boot process. Corresponds to C6x DSP bootmode #2.* *DSP MAP-0 memory map is used with ASYNC 32-bit CE-0 space.*	ON	ON	OFF	ON	ON	ON
BM#6 (HPI BOOT)	*Boot from HPI. Corresponds to C6x DSP bootmode #6.* *DSP MAP-0 memory map is used with ASYNC 32-bit CE-0 space. Requires optional setting of EMIF CE-0/CE-1/CE-2/CE-3 area configuration registers by host software via DSP HPI port.*	ON	OFF	OFF	ON	OFF	ON
BM#10 (FLASH BOOT)	*Boot from on-board 8-bit FLASH/EPROM. Corresponds to C6x DSP bootmode #10.* *DSP MAP-0 memory map is used with ASYNC 32-bit CE-0 space.*	OFF	ON	OFF	ON	ON	OFF

Note:
1. 'ON' corresponds to installed jumper and switched on switch; 'OFF' corresponds to removed jumper and switched off switch.
2. Not shown bootmode configurations are reserved and are not recommended for usage.
3. Highlighted configuration corresponds to the factory setting.

Bootmode configuration for *TORNADO-P64xx* on-board DSP is set by host PC application (via *HIF_DSP_BMODE_RG* register of host PCI-bus interface) in case on-board TMS320C64xx DSP is running in *host operation mode* (in case *TORNADO-P64xx* board is installed into host PCI-bus slot and *M_SA_MODE* bit of *HIF_CONTROL_RG* register of host PCI-bus interface is set to the '0' state in order DSP reset input can be controlled via host PC software via *M_GO* bit of *HIF_CONTROL_RG* register). However, in case on-board TMS320C64xx DSP is running in *stand-alone operation mode* (in case either *TORNADO-P64xx* board is either not installed into host PCI-bus slot, or in case *TORNADO-P64xx* board is installed into host PCI-bus slot and *M_SA_MODE* bit of *HIF_CONTROL_RG* register of host PCI-bus interface is set to the '1' state), then TMS320C64xx DSP bootmode configuration can be set via on-board SW2-1/2 switches. Table 2-2b provides details about how to configure bootmode for *TORNADO-P64xx* on-board TMS320C64xx DSP for DSP host operation mode and DSP stand-alone operation mode. Not shown DSP bootmode configurations are reserved and are not recommended for usage. Refer to section 'Host PCI-bus Interface' later in this chapter for more details about *HIF_DSP_BMODE_RG* and *HIF_CONTROL_RG* registers.

CAUTION

DSP bootmode configuration for *TORNADO-P64xx* DSP systems can be set via host PC software for DSP host mode only, and must be set via on-board SW2-1/2 switches in case DSP runs in stand-alone operation mode.

CAUTION

HIF_DSP_BMODE_RG register of *TORNADO-P64xx* host PCI-bus interface can be set by host PC software only while DSP is in the host operation mode (*TORNADO-P64xx* board is installed into host PCI-bus slot and *M_SA_MODE* bit of *HIF_CONTROL_RG* register of host PCI-bus interface is set to the '0' state) and DSP is in the reset state (*MGO* bit of *HIF_CONTROL_RG* register is in the '0' state).

Table 2-2b. TMS320C64xx DSP Bootmode Configurations for *TORNADO-P64xx*.

'C64xx DSP operation mode	**'C64xx DSP Bootmode**	**Description**	***HIF_DSP_BMODE_RG* register bits**		**on-board SW2 switch**	
			DSP_BMODE-0	***DSP_BMODE-1***	**SW2-1**	**SW2-2**
Host mode	*NO BOOT*	*No boot process.*	0	0	x	x
	HPI BOOT	*Boot from HPI port.*	1	0	x	x
	FLASH BOOT	*Boot from on-board 8-bit FLASH/EPROM memory.*	0	1	x	x
Stand-alone mode	*NO BOOT*	*No boot process.*	x	x	ON	ON
	HPI BOOT	*Boot from HPI port.*	x	x	OFF	ON
	FLASH BOOT	*Boot from on-board 8-bit FLASH/EPROM memory.*	x	x	ON	OFF

Note:
1. 'ON' corresponds to the switched on switch button; 'OFF' corresponds to the switched off switch button. 'X' corresponds to don't care state.
2. Not shown bootmode configurations are reserved and are not recommended for usage.
3. Highlighted configuration for *DSP host operation mode* is set as default on host PCI-bus reset condition in case TORNADO-P64xx board is installed into host PCI-bus slot. Highlighted configuration for *DSP stand-alone operation mode* corresponds to default factory switch setting.

In case '*NO BOOT*' DSP bootmode is selected, then DSP starts program execution from memory address 00000000H immediately after release of DSP reset signal. Note, that for *TORNADO-P62xx/P67* DSP systems, DSP memory address 00000000H corresponds to on-board DPRAM, whereas for *TORNADO-P64xx* DSP systems, DSP memory address 00000000H corresponds to DSP on-chip memory (see table 2-1). '*NO BOOT*' DSP bootmode is typically selected during debugging of DSP software via JTAG emulator, and is also default DSP bootmode for *TORNADO-P62xx/P67* DSP systems when board is installed into host PCI-bus slot, since all host PC utilities upload DSP code/data directly via *TORNADO-P62xx/P67* on-board DPRAM.

In case '*HPI BOOT*' DSP bootmode is selected, then DSP kernel is held in the reset state immediately after release of DSP reset signal while the remainder of the DSP devices is functional, including DSP on-chip HPI port. In '*HPI BOOT*' DSP bootmode, host PC software can access all DSP memory areas including DSP on-chip/off-chip memories and peripherals in order to upload code/data into DSP environment. However, accessing DSP off-chip memories (DPRAM, SBSRAM, SDRAM, etc) during '*HPI BOOT*' DSP bootmode requires that host PC software will at-first to correctly configure all DSP on-chip EMIF (EMIF-A/B for TMS320C64xx DSP) registers via DSP HPI port in accordance with table 2-3. DSP will start program execution from memory location at address 00000000H as soon as host PC software will set *DSPINT* bit of *HPIC* register (*HIF_HPIC_RG* register of *TORNADO-P6x* host PCI-bus interface, refer to section 'Host PCI-bus Interface' later in this chapter for more details). Although '*HPI BOOT*' DSP bootmode is a convenient method to access all DSP environment for initial DSP code upload, it is not generally used for *TORNADO-P62xx/P67* DSP systems, since *TORNADO-P64xx* COFF loaders are using DPRAM to upload code to all DSP memory areas. Instead, for *TORNADO-P64xx* DSP systems, '*HPI BOOT*' DSP bootmode is the only way to upload DSP

code/data into DSP start-up memory at address 00000000H, which is allocated to DSP on-chip memory, and is dynamically selected by all *TORNADO-P64xx* COFF loaders.

In case '*FLASH BOOT*' DSP bootmode is selected, then, after release of DSP reset signal, DSP will copy 64 Kbyte (*TORNADO-P62xx/P67*) or 1 Kbyte (*TORNADO-P64xx*) of on-board 8-bit FLASH/EPROM contents at the beginning of FLASH/EPROM memory to DSP memory at address 00000000H and will start program execution from memory location at address 00000000H as soon data copy is complete. Note, that copied 64 Kbyte FLASH/EPROM data contents is large enough for *TORNADO-P62xx/P67* DSP systems and can generally contain end-user application compiled with TI C6000 C/C++ compiler, whereas for *TORNADO-P64xx* boards, copied 1 Kbyte FLASH/EPROM data contents is tiny and can include only initial bootloader code compile using C6000 assembler only (minimum C-code application does not fit into 1 Kbyte size when compiled with TI C6000 C/C++ compiler). '*FLASH BOOT*' DSP bootmode is typically selected for stand-alone DSP operation mode after DSP application has been debugged and final code/data has been copied to on-board FLASH/EPROM memory.

TMS320C6x DSP operation modes and reset control

TORNADO-P6x on-board TMS320C6x DSP can run the following modes, which are defined by board installation and software configuration of *TORNADO-P6x* DSP system:

- *host PC operation mode*, which is set in case *TORNADO-P6x* DSP system is installed into host PCI-bus slot of host PC and *M_SA_MODE* bit of *HIF_CONTROL_RG* register of host PCI-bus interface is set to the '0' state (refer to section "Host PCI-bus Interface" later in this chapter for more details)
- *stand-alone operation mode*, which is set in the following cases:
  - in case *TORNADO-P6x* DSP system is installed into PCI-bus slot of host PC and *M_SA_MODE* bit of *HIF_CONTROL_RG* register of host PCI-bus interface is set to the '1' state (refer to section "Host PCI-bus Interface" later in this chapter for more details)
  - in case *TORNADO-P6x* DSP system case is not installed into PCI-bus slot of host PC, and external power is applied via on-board JP10 power connector.

Reset signal for *TORNADO-P6x* on-board TMS320C6x DSP can be generated from the following sources, which are defined by current DSP operation mode:

- *from host PCI-bus interface* using *M_GO* bit of *HIF_CONTROL_RG* register in case on-board TMS320C6x DSP is running in host PC operation mode
- *from on-board SW1 reset pushbutton* in case on-board TMS320C6x DSP is running in stand-alone operation mode
- *from on-board JP7 external DSP reset connector* in case on-board TMS320C6x DSP is running in stand-alone operation mode (refer to figure 2-7 and to the corresponding subsection below)
- *from on-board power monitor* on power on and power failure conditions in case on-board TMS320C6x DSP is running in stand-alone operation mode
- *on WDT expiration event* in case on-board TMS320C6x DSP is running in stand-alone operation mode and WDT is enabled via *DSP_WDT_EN_RG* IOX register (refer to the corresponding subsection below).

Setting EMIF control registers of TMS320C6x DSP

In order to provide correct operation of *TORNADO-P6x* on-board hardware, TMS320C6x DSP on-chip EMIF control registers shall be set by DSP application software in accordance with table 2-3a for *TORNADO-P62xx/P67* DSP systems and in accordance with table 2-3b for *TORNADO-P64xx* DSP systems.

For more details about TMS320C6x DSP EMIF control registers refer to original documentation for TI TMS320C6x DSP.

Table 2-3a. Recommended settings for EMIF control registers of TMS320C620x/C6701 DSP of *TORNADO-P62xx/P67* DSP systems.

TMS320C620x/C6701 DSP on-chip EMIF control register	***TORNADO-P62*** **(5ns DSP clock cycle)**	***TORNADO-P67*** **(6ns DSP clock cycle)**	***TORNADO-P6202*** **(4ns DSP clock cycle)**	***TORNADO-P6203*** **(3.3ns DSP clock cycle)**
EMIF Global Control Register (EMIF_GBLCTL)	0x3078 (for –5, –6, -7.5 and -10 speed grades of installed SBSRAM chips) [1)] 1/2x SBSRAM clk (1ws) 1/2x SDRAM clk (1ws) CLKOUT1/CLKOUT2 are enabled 0x307c (for –5 speed grade of installed SBSRAM chips) [1)] 1x SBSRAM clk (0ws) 1/2x SDRAM clk (1ws) CLKOUT1/CLKOUT2 are enabled	0x3078 (for –5, –6, -7.5 and -10 speed grades of installed SBSRAM chips) [1)] 1/2x SBSRAM clk (1ws) 1/2x SDRAM clk (1ws) CLKOUT1/CLKOUT2 are enabled 0x307c (for –5 and –6 speed grades of installed SBSRAM chips) [1)] 1x SBSRAM clk (0ws) [1)] 1/2x SDRAM clk (1ws) CLKOUT1/CLKOUT2 are enabled	0x3078 CLKOUT2 is enabled as 1/2x SBSRAM/SDRAM clock	0x3078 CLKOUT2 is enabled as 1/2x SBSRAM/SDRAM clock
EMIF CE-0 Space Control Register (EMIF_CE0CTL) *(area controls 32-bit DPRAM, DPSEM, PCIC, IOX, PIOX site, SIOX-A/B rev.C sites)*	0x31b3c623 32-bit ASYNC mode r/w strobe: 6 clk (30ns) r/w setup: 3 clk (15ns) r/w hold: 3 clk (15ns)	0x2162c522 32-bit ASYNC mode r/w strobe: 5 clk (30ns) r/w setup: 2 clk (12ns) r/w hold: 2 clk (12ns)	0x31f3c723 32-bit ASYNC mode r/w strobe: 7 clk (28ns) r/w setup: 3 clk (12ns) r/w hold: 3 clk (12ns)	0x4274c923 32-bit ASYNC mode r/w strobe: 9 clk (29ns) r/w setup: 4 clk (13ns) r/w hold: 3 clk (10ns)
EMIF CE-1 Space Control Register (EMIF_CE1CTL) *(area controls 8-bit EPROM/FLASH)*	0x8638d823 32-bit ASYNC mode r/w strobe: 24 clk (120ns) r/w setup: 8 clk (40ns) r/w hold: 3 clk (15ns)	0x8638d823 32-bit ASYNC mode r/w strobe: 24 clk (144ns) r/w setup: 8 clk (48ns) r/w hold: 3 clk (18ns)	0x87b8de23 32-bit ASYNC mode r/w strobe: 30 clk (120ns) r/w setup: 8 clk (32ns) r/w hold: 3 clk (12ns)	0xc93ce423 32-bit ASYNC mode r/w strobe: 36 clk (110ns) r/w setup: 12 clk (40ns) r/w hold: 3 clk (10ns)

EMIF CE-2 Space Control Register (EMIF_CE2CTL) *(area controls on-board SBSRAM for TORNADO-P62/P67 and on-board SBSRAM/SDRAM for TORNADO-P6202/P6203)*	0x40 32-bit SBSRAM mode	0x40 32-bit SBSRAM mode	0x40 32-bit SBSRAM mode (in case external memory is configures as SBSRAM) [2)] 0x30 32-bit SDRAM mode (in case external memory is configures as SDRAM) [2)]	0x40 32-bit SBSRAM mode (in case external memory is configures as SBSRAM) [2)] 0x30 32-bit SDRAM mode (in case external memory is configures as SDRAM) [2)]
EMIF CE-3 Space Control Register (EMIF_CE3CTL) *(area controls on-board SDRAM)*	0x30 32-bit SDRAM mode	0x30 32-bit SDRAM mode	0x40 32-bit SBSRAM mode (in case external memory is configures as SBSRAM) [2)] 0x30 32-bit SDRAM mode (in case external memory is configures as SDRAM) [2)]	0x40 32-bit SBSRAM mode (in case external memory is configures as SBSRAM) [2)] 0x30 32-bit SDRAM mode (in case external memory is configures as SDRAM) [2)]
EMIF SDRAM Control Register (EMIF_SDCTL)	0x07339000	0x07338000	0x07339000	0x0733a000
EMIF SDRAM Timing Register (EMIF_SDTIM)	1000	833	1250	1500

Notes:
1. Number of programmed wait states (either 0ws or 1ws) for on-board SBSRAM bank of *TORNADO-P62/P67* DSP systems depends upon the speed grade of installed SBSRAM chips. Contact MicroLAB Systems for information about the speed grade of installed SBSRAM chips.
2. External DSP memory for *TORNADO-P6202/P6203* DSP systems can be configured by DSP software as either SBSRAM or SDRAM via bit *XMEM* of *DSP_SYS_STAT_RG* IOX register. Refer to the corresponding subsection below for more details.

Table 2-3b. Recommended settings for EMIF control registers of TMS320C64xx DSP of *TORNADO-P64xx* DSP systems.

TMS320C64xx DSP on-chip EMIF control register	**EMIF area mode**	**value**
TMS320C64xx EMIF-A Control Registers		
EMIF-A Global Control Register (EMIFA_GBLCTL)	-	0x0001207c
EMIF-A CE-0 Space Control Register (EMIFA_CE0CTL) *(area controls 64-bit SBSRAM)*	64-bit SBSRAM	0x000000e0
EMIF-A CE-0 Space Secondary Control Register (EMIFA_CE0SEC)		0x00000002
EMIF-A CE-1 Space Control Register (EMIFA_CE1CTL) *(area controls 32-bit synchronous DPRAM)*	32-bit SBSRAM	0x00000040
EMIF-A CE-1 Space Secondary Control Register (EMIFA_CE1SEC)		0x00000002
EMIF-A CE-2 Space Control Register (EMIFA_CE2CTL) *(area controls 64-bit SDRAM)*	64-bit SDRAM	0x000000d0
EMIF-A CE-2 Space Secondary Control Register (EMIFA_CE2SEC)		0x00000002
EMIF-A CE-3 Space Control Register (EMIFA_CE3CTL) *(area is reserved)*	8-bit ASYNC (reserved)	0xffffff03
EMIF-A CE-3 Space Secondary Control Register (EMIFA_CE3SEC)		x
EMIF-A SDRAM Control Register (EMIFA_SDCTL)	-	0x57115000 (SDRAM 4Mx64) 0x63115000 (SDRAM 16Mx64)
EMIFA SDRAM Extension Register (EMIFA_SDEXT)	-	0x00014d29

EMIFA SDRAM Timing Register (EMIFA_SDTIM)	-	1562 (SDRAM 4Mx64) 781 (SDRAM 16Mx64)
TMS320C64xx EMIF-B Control Registers		
EMIF-B Global Control Register (EMIFB_GBLCTL)	-	0x0001207c
EMIF-B CE-0 Space Control Register (EMIFB_CE0CTL) *(area controls PCIC, IOX, SIOX-A/B rev.C sites)*	16-bit ASYNC	0x10d14311 r/w strobe: 3 clk (30ns) r/w setup: 1 clk (10ns) r/w hold: 1 clk (10ns)
EMIF-B CE-0 Space Secondary Control Register (EMIFB_CE0SEC)		x
EMIF-B CE-1 Space Control Register (EMIFB_CE1CTL) *(area controls 8-bit FLASH/EPROM)*	16-bit ASYNC (ROM)	0x23124c11 r/w strobe: 12 clk (120ns) r/w setup: 2 clk (20ns) r/w hold: 1 clk (10ns)
EMIF-B CE-1 Space Secondary Control Register (EMIFB_CE1SEC)		x
EMIF-B CE-2 Space Control Register (EMIFB_CE2CTL) *(area is reserved)*	8-bit ASYNC (reserved)	0xffffff03
EMIF-B CE-2 Space Secondary Control Register (EMIFB_CE2SEC)		x
EMIF-B CE-3 Space Control Register (EMIFB_CE3CTL) *(area controls PIOX/PIOX-16 DCM site)*	16-bit ASYNC (reserved)	0x10d14311 r/w strobe: 3 clk (30ns) r/w setup: 1 clk (10ns) r/w hold: 1 clk (10ns)
EMIF-B CE-3 Space Secondary Control Register (EMIFB_CE3SEC)		x
EMIF-B SDRAM Control Register (EMIFB_SDCTL)	-	x
EMIFB SDRAM Extension Register (EMIFB_SDEXT)	-	x
EMIFB SDRAM Timing Register (EMIFB_SDTIM)	-	x

Notes: 1. *TORNADO-P64xx* EMIF-A/B clock is 100 MHz (10 ns clock cycle).
2. 'X' denote don't care value.

CAUTION

EMIF clock for *TORNADO-P62xx/P67* on-board TMS320C620x/C6701 DSP is equal to the DSP clock and is 200 MHz for *TORNADO-P62*, 167 MHz for *TORNADO-P67*, 250 MHz for *TORNADO-P6202* and 300 MHz for *TORNADO-P6203*.

EMIF-A/B clock for *TORNADO-P64xx* on-board TMS320C64xx DSP is 100 MHz.

DPRAM memory area of TORNADO-P62xx/P67 DSP systems

TORNADO-P62xx/P67 on-board DPRAM is mapped to 00000000H memory base address (refer to table 2-1a) of on-board TMS320C620x/C6701 DSP, and is used for DSP start-up code and communication between DSP and host PCI-bus interface via 32-bit common memory area.

TORNADO-P62xx/P67 on-board DPRAM appears as standard 32-bit asynchronous memory and can be accessed by both DSP and host PCI-bus interface. *TORNADO-P62xx/P67* DSP systems are available with either 32Kx32 or 64Kx32 DPRAM capacity.

All accesses to *TORNADO-P62xx/P67* on-board DPRAM feature no arbitration delays for DSP and host PCI-bus interface unless both DSP and host PCI-bus interface are addressing the same DPRAM memory location. In the latter case there is no arbitration preferences, and the first accessing port will proceed without arbitration delay, whereas the other port will be pending until the first port will finish the access cycle. DPRAM access collision is resolved by means of DPRAM internal arbitration circuit.

TORNADO-P62xx/P67 on-board DPRAM area has two specific memory locations, which are known as *DPRAM_HM_RQ* and *DPRAM_MH_RQ*. These DPRAM locations provide PCI-to-DSP and DSP-to-PCI interrupt generation along with standard common memory functionality. Refer to the corresponding subsection below for more details.

DPRAM memory area of TORNADO-P64xx DSP systems

TORNADO-P64xx on-board DPRAM is mapped to EMIF-A CE-1 area of on-board TMS320C64xx DSP, and is used for high-speed communication between DSP and host PCI-bus interface via 32-bit common memory area. *TORNADO-P64xx* on-board DPRAM cannot be used for DSP start-up code, since this is TMS320C64xx DSP on-chip RAM, which is mapped to 00000000H memory base address.

TORNADO-P64xx on-board DPRAM appears as 32-bit synchronous dual-port memory and can be accessed by both DSP and host PCI-bus interface. *TORNADO-P64xx* DSP systems are available with either 128Kx32 or 256Kx32 DPRAM capacity.

TORNADO-P64xx on-board DPRAM is accessed by on-board DSP at full EMIF-A speed at 100 MHz thus providing maximum DSP external memory access performance. On host PCI-bus side, *TORNADO-P64xx* on-board DPRAM is accessed at maximum available PCI-bus speed (133 Mbyte/s) using ‘PCI-bus burst cycles’ without PCI-bus wait states.

TORNADO-P64xx on-board DPRAM is always accessed without arbitration delays for both DSP and host PCI-bus interface, even in case both DSP and host PCI-bus interface are addressing the same DPRAM memory

location. So, care must be taken by both host PC software and TMS320C64xx DSP software to ensure that they both are not writing simultaneously to the same DPRAM location.

TORNADO-P64xx DSP systems with 256Kx32 on-board DPRAM provide two specific memory locations, which are known as *DPRAM_HM_RQ* and *DPRAM_MH_RQ*. These DPRAM locations provide PCI-to-DSP and DSP-to-PCI interrupt generation along with standard common memory functionality. Refer to the corresponding subsection below for more details.

CAUTION

DPRAM_HM_RQ and *DPRAM_MH_RQ* specific DPRAM memory locations, which generate PCI-to-DSP and DSP-to-PCI interrupt requests correspondingly, are available for *TORNADO-P64xx* DSP systems with 256Kx32 DPRAM only..

TORNADO-P64xx DSP systems with 128Kx32 on-board DPRAM do not provide *DPRAM_HM_RQ* and *DPRAM_MH_RQ* specific DPRAM memory locations.

Generating PCI-to-DSP and DSP-to-PCI interrupt requests via DPRAM

TORNADO-P62xx/P67 on-board DPRAM and *TORNADO-P64xx* DSP systems with 256Kx32 on-board DPRAM provide two specific memory locations, which are known as *DPRAM_HM_RQ* and *DPRAM_MH_RQ* and which provide PCI-to-DSP and DSP-to-PCI interrupt generation along with standard common DPRAM memory functionality.

DPRAM_HM_RQ and *DPRAM_MH_RQ* DSPRAM memory locations are allocated at the DPRAM addresses in accordance with table 2-1 and can be used for generation of PCI-to-DSP and DSP-to-PCI interrupt requests correspondingly along with passing the 32-bit interrupt request code via these DPRAM memory cells. This method is similar to the mailboxes of on-board S5933 PCIC controller and delivers one more path of mutual interrupt generation into communication between host PCI-bus and DSP.

CAUTION

When host PCI-bus writes to the *DPRAM_HM_RQ* address, then active *DSP_DPRAM_IRQ* interrupt request is generated to the DSP environment. This interrupt request remains active until DSP will read contents of this DPRAM memory location. Writing to this DPRAM location from the DSP side does not effect the state of *DSP_DPRAM_IRQ* interrupt request.

The *DSP_DPRAM_IRQ* interrupt request can generate active DSP interrupt request in case it is routed via the corresponding interrupt request selector to any of DSP external interrupt requests or DSP NMI. Refer to the corresponding subsection later in this section for more details about external DSP interrupt generation.

CAUTION

When DSP writes to the *DPRAM_MH_RQ* address, then active *PCI_DPRAM_IRQ* interrupt request is generated to the PCI-bus. This interrupt request remains active until host PCI-bus will read contents of this DPRAM memory location. Writing to this DPRAM location from the host PCI-bus side does not effect the state of *PCI_DPRAM_IRQ* interrupt request.

The *PCI_DPRAM_IRQ* interrupt request can generate active PCI-bus interrupt request in case it is enabled via the HIF interrupt mask register. Refer to section "Host PCI-bus Interface" later in this chapter for more details.

DPSEM area for TORNADO-P62xx/P67 DSP systems

TORNADO-P62xx/P67 DSP systems provide on-board dual-port hardware semaphores (DPSEM) area, which is accessible by both DSP and host PCI-bus interface. Hardware semaphores are useful for synchronizing access to any shared resources (DPRAM, etc) and setting synchro-events between DSP and host PCI-bus.

CAUTION

TORNADO-P64xx DSP systems do not provide on-board dual-port hardware semaphores (DPSEM) area.

DPSEM area is a part of asynchronous EMIF CE-0 area of *TORNADO-P62xx/P67* on-board TMS320C620x/C6701 DSP, and appears as eight 32-bit hardware semaphores. Access to the DPSEM area is performed without any arbitration delays on DSP and PCI-bus sides.

Each semaphore occupies bit D0 only within its 32-bit data word (bits D1..D31 are an extended copy of bit D0), and has only two valid states: '0' and '1'. The semaphore logic is active low, and the '0' state is called as 'open state' of semaphore (semaphore token), whereas the '1' state is called as 'closed state' of semaphore. Hardware semaphore logic guarantees that both ports will never get enable state (or semaphore token) simultaneously. Table 2-4 provides example of DPSEM semaphore procurement sequence for *TORNADO-P62xx/P67* DSP systems.

Table 2-4. Example of the DPSEM semaphore procurement sequence for *TORNADO-P62xx/P67* DSP systems.

Function	semaphore D0 data at the PCI-bus port	semaphore D0 data at the DSP port	Status
No action.	1	1	Semaphores are closed. Default initial state.
PCI-bus writes '0' to semaphore.	0	1	PCI-bus receives open semaphore.
DSP writes '0' to semaphore.	0	1	No change. DSP has to wait for semaphore to be released by the PCI-bus.
PCI-bus writes '1' to semaphore.	1	0	PCI-bus releases semaphore, and DSP receives open semaphore.
PCI-bus writes '0' to semaphore.	1	0	No change. PCI-bus has to wait for semaphore to be released by the DSP.
DSP writes '1' to semaphore.	0	1	DSP releases semaphore, and PCI-bus receives open semaphore.
PCI-bus writes '1' to semaphore.	1	1	PCI-bus releases semaphore, and semaphores are now closed.

CAUTION

TORNADO-P6x DSP systems do not perform default setting of dual-port hardware semaphores (DPSEM) to the 'close' state on host PC reset and DSP reset condition.

Both host PC application and DSP application shall reset dual-port hardware semaphores of *TORNADO-P6x* DSP systems to default 'close' state prior semaphores will be used by either host PC or DSP application.

SBSRAM and SDRAM memory areas for TORNADO-P62xx/P67 DSP systems

TORNADO-P62xx/P67 DSP systems provide on-board 32-bit SBSRAM bank for external DSP program/data, which features 128K/512K/1Mx32 (0.5/2/4 Mbytes) capacity and is allocated into EMIF CE-2 area of on-board TMS320C620x/C6701 DSP.

TORNADO-P62/P67 DSP systems provide on-board 32-bit SDRAM bank for external DSP program/data, which features 4Mx32 (16 Mbytes) capacity and is allocated into EMIF CE-3 area of on-board TMS320C620x/C6701 DSP.

TORNADO-P6202/P6203 DSP systems provide two on-board 32-bit SDRAM banks for external DSP program/data. Each SDRAM bank features 4Mx32 (16 Mbytes) capacity. Primary SDRAM bank of *TORNADO-P6202/P6203* DSP systems is allocated into EMIF CE-3 area of on-board TMS320C6202/C6203 DSP, whereas both secondary SDRAM bank and on-board SBSRAM bank share common EMIF CE-2 area of on-board TMS320C6202/C6203 DSP.

CAUTION

Both SBSRAM and SDRAM memory banks of *TORNADO-P62xx/P67* DSP systems are optional and are installed in accordance with the customer specification when purchasing the product.

CAUTION

TORNADO-P62/P67 DSP systems support on-board SBSRAM and SDRAM simultaneously, i.e. on-board TMS320C6201/TMS320C6701 DSP can access both SBSRAM and SDRAM without EMIF re-configuration.

TORNADO-P6202/P6203 DSP systems do not support on-board SBSRAM and SDRAM simultaneously. On-board TMS320C6202/TMS320C6203 DSP can be configured by DSP software to access either external SBSRAM or external SDRAM by means of appropriate configuration of DSP on-chip EMIF control registers (table 2-3) and selection of external memory type via bit *XMEM* of *DSP_SYS_STAT_RG* register (refer to the corresponding subsection below).

CAUTION

TORNADO-P62/P67 on-board SBSRAM bank can be configured by on-board DSP software to run either with 0ws or 1ws depending upon the particular SBSRAM memory chips installed. Number of wait states for accessing on-board SBSRAM can be programmed via *SSCRT* bit of TMS320C6201/C6701 DSP on-chip EMIF global control register (*EMIF_GCR*) in accordance with table 2-3.

TORNADO-P6202/P6203 on-board SBSRAM bank always run at 1/2x DSP clock rate and provides 1ws when accessed by on-board DSP.

CAUTION

TORNADO-P62xx/P67 on-board SDRAM bank(s) always run at 1/2x DSP clock rate and provide(s) 1ws when accessed by on-board TMS320C620x/C6701 DSP.

SBSRAM and SDRAM memory areas for TORNADO-P64xx systems

TORNADO-P64xx DSP systems provide on-board 64-bit SBSRAM and SDRAM memory banks for external DSP program/data, which are allocated to EMIF-A CE-0 and CE-2 areas of on-board TMS320C64xx DSP.

TORNADO-P64xx on-board SBSRAM memory bank features 128K/256K/512Kx64 (1/2/4 Mbytes) capacity, whereas SDRAM memory bank provides 4M/16Mx64 (32/128 Mbytes) capacity.

CAUTION

Both SBSRAM and SDRAM memory banks of *TORNADO-P64xx* DSP systems are optional and are installed in accordance with the customer specification when purchasing the product.

Both SBSRAM and SDRAM memory banks of *TORNADO-P64xx* DSP systems run at 100 MHz synchronous memory clock thus delivering maximum of available DSP performance when accessing external memory.

CAUTION

TORNADO-P64xx DSP systems support on-board SBSRAM and SDRAM memories simultaneously, i.e. on-board TMS320C64xx DSP can access both SBSRAM and SDRAM without EMIF re-configuration.

FLASH/EPROM memory area

On-board 8-bit FLASH/EPROM of *TORNADO-P6x* DSP systems is included for optional easy migration from PC plug-in applications to stand-alone applications.

On-board FLASH/EPROM bank is allocated into EMIF CE-1 area of on-board TMS320C620x/C6701 DSP for *TORNADO-P62xx/P67* DSP systems (table 2-1a) and into EMIF-B CE-1 area of on-board TMS320C64xx DSP for *TORNADO-P64xx* DSP systems (table 2-1b), and can be used for DSP bootload during DSP stand-alone operation mode (table 2-2) and to store non-volatile data.

CAUTION

TORNADO-P6x DSP systems have been designed to install either 5v-only 128K/512Kx8 FLASH memory chips or 128K..1Mx8 EPROM memory chips in PLCC-32 IC package and less than 100ns access time into dedicated on-board S1 socket (fig.2-2 and A-1).

Recommended 5v-only FLASH memory chips are available from AMD and other vendors. Contact MicroLAB Systems for a complete list of compatible FLASH/EPROM memory chip vendors.

Installation of other FLASH/EPROM memory chips than that specified in table 2-3 may result in damage of FLASH/EPROM chip and/or of *TORNADO-P6x* hardware.

TORNADO-P6x DSP systems do not provide on-board facility for programming 8-bit EPROM chips, whereas 8-bit 5v-only FLASH memory chips can be programmed directly by on-board DSP using corresponding FLASH programming utilities (FLASH programming utilities for on-board TMS320C6x DSP are provided as standard with *TORNADO-P6x* DSP systems). Once 5v-only FLASH chip is installed, then it can be programmed either by DSP software and via host PCI-bus memory interface. The EPROM chip, however, can be programmed in the external programmer only, and can be used for read-only bootload purpose in *TORNADO-P6x* DSP systems.

The on-board J3 jumper set (*TORNADO-P62/P67*) and on-board SW3 switch (*TORNADO-P6202/P6203/P64xx*)are used to select the particular FLASH/EPROM chip type and to set the write protect features for the FLASH chips in accordance with table 2-5.

Table 2-5. FLASH/EPROM chip selector.

FLASH/EPROM chip in PLCC-32 IC package	**J3 jumper set configuration (*TORNADO-P62/P67*) SW3 switch configuration (*TORNADO-P6202/P6203/P64xx*)**					
	J3-1 SW3-1	**J3-2 SW3-2**	**J3-3 SW3-3**	**J3-4 SW3-4**	**J3-5 SW3-5**	**J3-6 SW3-6**
AMD Am29F010B 128Kx8 FLASH *AMD Am29F040B 512Kx8 FLASH* *with WRITE ENABLE*	OFF	ON	OFF	ON	OFF	OFF
AMD Am29F010B 128Kx8 FLASH *AMD Am29F040B 512Kx8 FLASH* *with WRITE DISABLE*	OFF	ON	OFF	OFF	ON	OFF
generic 27C010 128Kx8 EPROM *generic 27C020 256Kx8 EPROM*	OFF	OFF	ON	OFF	ON	OFF
generic 27C040 512Kx8 EPROM	OFF	OFF	ON	OFF	OFF	ON
generic 27C080 1Mx8 EPROM	ON	OFF	OFF	OFF	OFF	ON

Notes:.
1. The highlighted configuration corresponds to the factory setting.
2. The recommended access time for the FLASH/EPROM chip is 100ns or less.

CAUTION

TORNADO-P62xx/P67xx on-board TMS320C620x/C6701 DSP allocates 8-bit FLASH/EPROM data words on 32-bit data word boundaries.

TORNADO-P64xx on-board TMS320C64xx DSP allocates 8-bit FLASH/EPROM data words on 16-bit data word boundaries.

TMS320C620x/C6701 DSP on-chip EMIF CE-1 control register for *TORNADO-P62xx/P67* DSP systems and TMS320C64xx DSP on-chip EMIF-B CE-1 control register for *TORNADO-P64xx* DSP systems shall be set in accordance with tables 2-3a and 2-3b correspondingly in order to correctly access on-board FLASH/EPROM memory.

FLASH memory bank provides FLASH memory write protection by means of J3-4 (SW3-4) and J3-5 (SW3-5) jumpers/switches in order to exclude unauthorized FLASH memory data update.

CAUTION

If J3-5 jumper is removed (SW3-5 switch is set to OFF) and J3-4 jumper is installed (SW3-4 switch is set to ON) while the FLASH memory chip is installed, then the FLASH memory can be programmed either by DSP software or via host PCI-bus memory interface.

If J3-5 jumper is installed (SW3-5 switch is set to ON) and J3-4 jumper is removed (SW3-4 switch is set to OFF) while the FLASH memory chip is installed, then writing to FLASH memory is disabled.

S5933 PCIC AOB operation registers area

TORNADO-P6x on-board TMS320C6x DSP can access add-on-bus (AOB) operation registers of *TORNADO-P6x* on-board AMCC S5933 PCIC, which is the part of *TORNADO-P6x* host PCI-bus interface.

AMCC S5933 PCIC on-chip 32-bit AOB operation registers are directly mapped into DSP PCIC sub-area of asynchronous EMIF CE-0 area of on-board TMS320C620x/C6701 DSP for *TORNADO-P62xx/P67* DSP systems (table 2-1a) and of EMIF-B CE-0 area of on-board TMS320C64xx DSP for *TORNADO-P64xx* DSP systems (table 2-1b), and are used for communication between DSP and host PCI-bus and to control PCI-bus mastering transfers from the DSP environment.

CAUTION

This subsection contains brief information about AMCC S5933 PCIC on-chip AOB operation registers.

For more details about *TORNADO-P6x* on-board AMCC S5933 PCIC refer to Appendix B of this manual and to original AMCC S5933 PCIC User's Guide, which is included in either paper or electronic form along with this manual.

CAUTION

TORNADO-P6x DSP PCIC area, which comprises of AMCC S5933 PCIC on-chip AOB operation registers, can be accessed by *TORNADO-P6x* on-board DSP only.

DSP PCIC area comprises of the following 32-bit AMCC S5933 PCIC on-chip AOB operation registers:

- *DSP_PCIC_FIFO_RG* (PCIC read/write FIFO) registers (read: read-FIFO, write: write-FIFO)
- *DSP_PCIC_AMBEF_RG* (PCIC Add-on Mailbox Empty/Full Status) register (read-only)
- *DSP_PCIC_AINT_RG* (PCIC Add-on Interrupt Control) register (read/write)
- *DSP_PCIC_AGCSTS_RG* (PCIC Add-on General Control and Status) register (read/write)
- *DSP_PCIC_MWAR_RG* (PCIC PCI-bus Master Write Address) register (read/write)
- *DSP_PCIC_MWTC_RG* (PCIC PCI-bus Master Write Transfer Counter) register (read/write)
- *DSP_PCIC_MRAR_RG* (PCIC PCI-bus Master Read Address) register (read/write)
- *DSP_PCIC_MRTC_RG* (PCIC PCI-bus Master Read Transfer Counter) register (read/write)
- *DSP_PCIC_IMBX0_RG..DSP_PCIC_IMBX3_RG* (PCIC Add-on Incoming Mailbox Registers #1..#4) registers (read-only)
- *DSP_PCIC_OMBX0_RG.. DSP_PCIC_OMBX3_RG* (PCIC Add-on Outgoing Mailbox Registers #1..#4) registers.

CAUTION

TMS320C6x DSP of *TORNADO-P6x* provides access to only those AMCC S5933 PCIC AOB operation registers, which are indicated above and in table 2-1.

AMCC S5933 PCIC internal (on-chip) addresses for AOB operation registers are automatically converted by *TORNADO-P6x* on-board hardware when DSP performs access to PCIC AOB operation registers in accordance with DSP address in table 2-1.

CAUTION

For details about AMCC S5933 PCIC on-chip AOB register formats refer to Appendix B of this manual and to AMCC S5933 PCIC User's Guide, which is supplied in either paper or electronic form along with this manual.

CAUTION

Access from TMS320C6x DSP to all AMCC S5933 PCIC AOB operation registers, except for *DSP_PCIC_FIFO_RG* register, might be performed using either 8-bit (byte), 16-bit and 32-bit datawords.

Access from TMS320C6x DSP to *DSP_PCIC_FIFO_RG* AOB operation register of AMCC S5933 PCIC is performed using 32-bit datawords only.

CAUTION

All accesses from TMS320C6x DSP to AOB operation registers of AMCC S5933 PCIC are performed with extra wait states as indicated in table 2-1, which depend upon the current host PCI-bus interface operation and eventual synchronization between the PCI-bus clock and DSP clock.

32-bit read/write *DSP_PCIC_FIFO_RG* PCIC AOB operation register is used for 'stream'-type bidirectional communication between *TORNADO-P6x* on-board DSP and host PCI-bus via 8-level bidirectional FIFO (first-in/first-out). When host PC application writes to *HOST_PCIC_FIFO_RG* AMCC S5933 PCIC on-chip PCI operation register of host PCI-bus interface (refer to Appendix B of this manual and to section "Host PCI-bus Interface" later in this chapter), then written data is put into host-to-DSP 8-level FIFO queue and DSP can read transferred data via *DSP_PCIC_FIFO_RG* PCIC on-chip AOB operation register using first-in/first-out algorithm. Once data has been read from FIFO, then it is lost and internal FIFO data is shifted. Vice-versa, when DSP writes to *DSP_PCIC_FIFO_RG* PCIC AOB operation register, then written data is put into DSP-to-host 8-level FIFO queue and host PC application can read transferred data from *HOST_PCIC_FIFO_RG* AMCC S5933 PCIC on-chip PCI operation register of host PCI-bus interface using first-in/first-out algorithm.

CAUTION

Before reading/writing from/to *DSP_PCIC_FIFO_RG* PCIC on-chip AOB operation register, *TORNADO-P6x* on-board DSP must check FIFO status via *DSP_PCIC_AGCSTS_RG* PCIC on-chip AOB operation register, or via *DSP_FIFO_STAT_RG* IOX register (refer to the corresponding subsection below for more details) in order to ensure that read FIFO contains valid data and that write FIFO has at least one empty location.

PCIC FIFO status flags can be cleared either by DSP via *DSP_PCIC_AGCSTS_RG* PCIC on-chip AOB operation register, or by host PC application via *HOST_PCIC_MCSR_RG* register of host PCIC area of host PCI-bus interface.

DSP_PCIC_FIFO_RG PCIC on-chip AOB operation register is also used DSP-to-host and host-to-DSP data transfers during DSP controlled PCI-bus mastering mode (refer to the corresponding subsection below for more details).

Read-only *DSP_PCIC_IMBX0_RG..DSP_PCIC_IMBX3_RG* PCIC on-chip AOB operation registers are used as 32-bit input mailboxes for data transfer from host PC application to *TORNADO-P6x* on-board DSP. *DSP_PCIC_IMBX0_RG..DSP_PCIC_IMBX3_RG* PCIC on-chip AOB operation registers are alias for AIB1..AIMB4 PCIC AOB operation registers correspondingly. When host PC application writes to any of *HOST_PCIC_OMBX0_RG.. HOST_PCIC_OMBX3_RG* AMCC S5933 PCIC on-chip PCI outgoing mailbox operation register of host PCI-bus interface (refer to Appendix B of this manual and to section "Host PCI-bus Interface" later in this chapter), then DSP can read written data via corresponding *DSP_PCIC_IMBX0_RG..DSP_PCIC_IMBX3_RG* PCIC on-chip AOB operation register. DSP can read *DSP_PCIC_IMBXn_RG* AOB incoming mailbox registers as many times as required by DSP application without loosing incoming mailbox register data, however PCI AOB incoming mailbox data ready flags, which are available via *DSP_PCIC_AMBEF_RG* PCIC on-chip AOB operation register, will be reset after first read from *DSP_PCIC_IMBXn_RG* PCIC on-chip AOB operation register.

Read/write *DSP_PCIC_OMBX0_RG..DSP_PCIC_OMBX3_RG* PCIC on-chip AOB operation registers are used as 32-bit outgoing mailboxes for data transfer from *TORNADO-P6x* on-board DSP to host PC application. *DSP_PCIC_OMBX0_RG..DSP_PCIC_OMBX3_RG* PCIC on-chip AOB operation registers are alias for AOB1..AOMB4 PCIC on-chip AOB operation registers correspondingly. When DSP writes to any of *DSP_PCIC_OMBX0_RG..DSP_PCIC_OMBX3_RG* PCIC on-chip AOB operation register, then host PC application read written data via corresponding read-only *HOST_PCIC_IMBX0_RG..HOST_PCIC_IMBX3_RG* AMCC S5933 PCIC on-chip PCI operation registers of host PCI-bus interface (refer to Appendix B of this manual and to section "Host PCI-bus Interface" later in this chapter). DSP can read back *DSP_PCIC_OMBXn_RG* PCIC on-chip AOB outgoing mailbox registers without loosing register data, and host PC application can read *HOST_PCIC_IMBXn_RG* AMCC S5933 PCIC on-chip PCI incoming mailbox operation registers of host PCI-bus interface as many times as required by host application without loosing incoming mailbox register data, however host PCI-bus incoming mailbox data ready flags, which are available via *HOST_PCIC_MBEF_RG* AMCC S5933 PCIC on-chip PCI operation register of host PCI-bus interface, will be reset after first read from *HOST_PCIC_IMBXn_RG* AMCC S5933 PCIC on-chip PCI operation register of host PCI-bus interface.

CAUTION

TORNADO-P6x on-board AMCC S5933 PCIC is configured with byte #3 of *DSP_PCIC_OMBX3_RG* outgoing mailbox register being used for generation of host PCI-bus interrupt.

This results in masking out most significant byte data when DSP writes to *DSP_PCIC_OMBX3_RG* PCIC on-chip AOB operation register, and in undefined returned data for most significant byte data when DSP reads from *DSP_PCIC_OMBX3_RG* PCIC on-chip AOB operation register.

Refer to Appendix B of this manual, original documentation for AMCC S5933 PCIC, the corresponding subsection below and to section "Host PCI-bus Interface" later in this chapter for more details.

DSP_PCIC_MWAR_RG, DSP_PCIC_MRAR_RG, DSP_PCIC_MWTC_RG and *DSP_PCIC_MRTC_RG* PCIC on-chip AOB operation registers shall be used by *TORNADO-P6x* on-board DSP in order to configure DSP controlled PCI-bus mastering (refer to the corresponding subsection below for more details).

DSP_PCIC_AINT_RG PCIC on-chip AOB operation register must be used to configure and control host-to-DSP AOB interrupt request from AMCC S5933 PCIC to *TORNADO-P6x* on-board DSP (for more details refer to Appendix B of this manual and to original AMCC S5933 PCIC User's Guide).

DSP_PCIC_AGCSTS_RG PCIC on-chip AOB operation register must be used to monitor PCIC FIFO status, clear FIFO flags, and to control access to *TORNADO-P6x* on-board PCIC configuration NvRAM (EEPROM) (for more details refer to Appendix B of this manual and to original AMCC S5933 PCIC User's Guide).

PIOX/PIOX-16 DCM site parallel interface area

TORNADO-P6x DSP systems provide universal 16-/32-bit parallel I/O expansion DCM site (PIOX/PIOX-16) for installation of compatible AD/DA/DIO and DSP coprocessor DCM.

PIOX/PIOX-16 DCM site interface area can be directly accessed by on-board TMS320C6x DSP. PIOX/PIOX-16 DCM site interface area occupies 512Kx32 sub-area of DSP memory map and is allocated into the corresponding sub-area of asynchronous EMIF CE-0 area of on-board TMS320C620x/C6701 DSP for *TORNADO-P62xx/P67* DSP systems (table 2-1a) and into EMIF-B CE-3 area of on-board TMS320C64xx DSP for *TORNADO-P64xx* DSP systems (table 2-1b).

PIOX/PIOX-16 DCM site interface comprises of TMS320C6x DSP data and address buses, data strobes, DSP-on-chip timers, external interrupt requests and power supply lines.

For more information about *TORNADO-P6x* on-board PIOX/PIOX-16 DCM site refer to section "Parallel I/O Expansion DCM Site (PIOX)" later in this chapter.

SIOX rev.B DCM site

TORNADO-P6x DSP systems provide on-board JP4 SIOX-A (serial I/O expansion interface) rev.B DCM site header (refer to figure 2-2 and A-1) for compatible *TORNADO* SIOX rev.B AD/DA/DIO and application specific DSP coprocessor DCM.

SIOX rev.B DCM site comprises of two serial ports, timer/IO pins, external interrupt requests, dedicated reset signal and ±5v/±12v power supply lines. For more details about SIOX-A rev.B DCM sites refer to section "Serial I/O Expansion DCM Sites (SIOX)" later in this chapter.

SIOX rev.C enhanced DCM site and SIOX rev.C DCM site parallel interface areas

TORNADO-P6x DSP systems provide two on-board serial I/O expansion revision C DCM sites (SIOX rev.C) SIOX-A (JP2) and SIOX-B (JP3) with for installation of compatible AD/DA/DIO and application specific DSP coprocessor DCM.

SIOX rev.C DCM site is an enhanced version of SIOX rev.B DCM site and comprises of two serial ports, timer/IO pins, external interrupt request, 8-bit DSP parallel data bus, 6-bit DSP address lines, parallel data strobes, dedicated reset signal and +5v/±12v power supply lines.

8-bit parallel data bus of SIOX-A/B rev.C DCM sites interface controlled by *TORNADO-P6x* on-board TMS320C6x DSP. Parallel 8-bit interface of each SIOX rev.C DCM site occupies least significant byte of 64x 32-bit words sub-area and is allocated into the corresponding sub-area of asynchronous EMIF CE-0 area of on-board TMS320C620x/C6701 DSP for *TORNADO-P62xx/P67* DSP systems (table 2-1a) and of EMIF-B CE-0 area of on-board TMS320C64xx DSP for *TORNADO-P64xx* DSP systems (table 2-1b).

For more information about *TORNADO-P6x* on-board SIOX rev.C DCM sites refer to section "Serial I/O Expansion DCM Sites (SIOX)" later in this chapter.

IOX registers area

TMS320C6x DSP environment of *TORNADO-P6x* DSP systems includes I/O expansion (IOX) registers area, which comprises of a set of control registers used for control of *TORNADO-P6x* on-board external DSP environment.

DSP IOX registers area is mapped into the corresponding sub-area of asynchronous EMIF CE-0 area of on-board TMS320C620x/C6701 DSP for *TORNADO-P62xx/P67* DSP systems (table 2-1a) and of EMIF-B CE-0 area of on-board TMS320C64xx DSP for *TORNADO-P64xx* DSP systems (table 2-1b).

DSP IOX registers area can be accessed by on-board TMS320C6x DSP only and is not visible from host PCI-bus memory interface. Memory addresses for IOX registers are listed in tables 2-1a and 2-b, and data formats are presented below in this section.

DSP IOX registers area includes the following registers:

- *DSP_FIFO_STAT_RG* read-only register (PCIC FIFO status)
- *DSP_AMWREN_RG* register (PCI-bus mastering control)
- *DSP_XIO_FMT_RG* register (external I/O data access format control, *TORNADO-P64xx* only)
- *DSP_MH_RQ_RG* write-only register (DSP-to-PCI request)
- *DSP_HM_RQ0_RG* and *DSP_HM_RQ1_RG* read-only registers (PCI-to-DSP requests)
- *DSP_PXSX_RESET_RG* register (software reset control for SIOX/PIOX DCM sites)

- *DSP_SYS_STAT_RG* register (system status/control), which is read-only for *TORNADO-P62/P67* DSP systems and read/write for *TORNADO-P6202/P6203* DSP systems
- *DSP_DEV_ID_RG* read-only register (device ID) for *TORNADO-P6202/P6203* DSP systems
- *DSP_NMI_SEL_RG* register (DSP NMI non-maskable interrupt source selector)
- *DSP_EXT_INT4_SEL_RG..DSP_EXT_INT7_SEL_RG* registers (DSP EXT_INT4..7 external interrupt source selector)
- *DSP_WDT_EN_RG* register (WDT enable feature)
- *DSP_WDT_CLR_RG* read-only (clear/reset WDT).

CAUTION

DSP IOX registers occupy bits D0..D3 of 32-bit DSP datawords for *TORNADO-P62xx/P67* DSP systems with bits D4..D31 ignored during writes and returned as undefined during reads.

DSP IOX registers for *TORNADO-P62xx/P67* DSP systems can be accessed either as 8-bit, or 16-bit, or 32-bit datawords without degradation of overall DSP performance.

CAUTION

DSP IOX registers occupy bits D0..D7 (least significant byte) of 32-bit DSP datawords for *TORNADO-P64xx* DSP systems with bits D8..D31 ignored during writes and returned as undefined during reads.

DSP IOX registers for *TORNADO-P64xx* DSP systems shall be accessed either as 8-bit, or 16-bit datawords without degradation of overall DSP performance.

Access of DSP IOX registers for *TORNADO-P64xx* DSP systems as 32-bit datawords is not recommended, since it will result in extra false TMS320C64xx DSP EMIF-B access cycle, which will result in degradation of overall DSP performance.

DSP_FIFO_STAT_RG IOX register

DSP_FIFO_STAT_RG IOX register is the read-only register, which reflects the current status of S5933 PCIC on-chip FIFO, which is used for communication between DSP and host PCI-bus interface and during PCI-bus mastering from DSP environment.

DSP_FIFO_STAT_RG IOX register (read-only)
(TORNADO-P62xx/P67)

X	*x*	*x*	*x*	*x*	*RFIFO_FF (r)*	*RFIFO_EF (r)*	*WFIFO_EF (r)*	*WFIFO_FF (r)*
bit-31...bit-8	Bit-7	Bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

DSP_FIFO_STAT_RG IOX register (read-only)
(TORNADO-P64xx)

X	*0*	*0*	*0*	*0*	*RFIFO_FF (r)*	*RFIFO_EF (r)*	*WFIFO_EF (r)*	*WFIFO_FF (r)*
bit-31...bit-8	Bit-7	Bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-6 provides details about *DSP_FIFO_STAT_RG* IOX register bits.

Table 2-6. Register bits of *DSP_FIFO_STAT_RG* IOX register.

Register bits	access mode	Value on DSP reset	Description
WFIFO_FF	r	-	Status of the full flag for DSP write FIFO (DSP-to-PCI FIFO of S5933 PCIC). *WFIFO_FF* =0 indicates that DSP write FIFO is not full and there are still empty locations in DSP write FIFO. DSP software can write to DSP write FIFO, whereas host PC software can read from DSP write FIFO in case bit D5 of *PCIC_MCSR_RG* register of host PCI-bus interface is in the '0' state (refer to section "Host PCI-bus Interface" later in this chapter and AMCC S5933 PCIC User's Guide for more details). *WFIFO_FF* =1 indicates that DSP write FIFO is full, i.e. it contains eight 32-bit words transferred from DSP to host PCI-bus). Further writes to DSP write FIFO by on-board DSP are not allowed, whereas host PC software can read from DSP write FIFO while bit D5 of *PCIC_MCSR_RG* register of host PCI-bus interface is in the '0' state (refer to section "Host PCI-bus Interface" later in this chapter and AMCC S5933 PCIC User's Guide for more details).

WFIFO_EF	r	-	Status of the empty flag for DSP write FIFO (DSP-to-PCI FIFO of S5933 PCIC). *WFIFO_EF* =0 indicates that DSP write FIFO is not empty and there is valid unread data in DSP write FIFO. DSP software can write to DSP write FIFO in case *WFIFO_FF* bit is in the '0' state, whereas host PC software can read from DSP write FIFO while bit D5 of *PCIC_MCSR_RG* register of host PCI-bus interface is in the '0' state (refer to section "Host PCI-bus Interface" later in this chapter and AMCC S5933 PCIC User's Guide for more details). *WFIFO_EF* =1 indicates that DSP write FIFO is empty, i.e. it does not contain valid data transferred from DSP to host PCI-bus. DSP software can write to DSP write FIFO while *WFIFO_FF* bit is in the '0' state, whereas further reads from DSP write FIFO by host PC are not allowed while bit D5 of *PCIC_MCSR_RG* register of host PCI-bus interface is in the '1' state (refer to section "Host PCI-bus Interface" later in this chapter and AMCC S5933 PCIC User's Guide for more details).
RFIFO_FF	r	-	Status of the full flag for DSP read FIFO (PCI-to-DSP FIFO of S5933 PCIC). *RFIFO_FF* =0 indicates that DSP read FIFO is not full and there are still empty locations in DSP read FIFO. DSP software can read from DSP read FIFO in case *RFIFO_EF* flag is in the '0' state, whereas host PC software can write to DSP read FIFO while bit D0 of *PCIC_MCSR_RG* register of host PCI-bus interface is in the '0' state (refer to section "Host PCI-bus Interface" later in this chapter and AMCC S5933 PCIC User's Guide for more details). *RFIFO_FF* =1 indicates that DSP write FIFO is full, i.e. it contains eight 32-bit words transferred from host PCI-bus to DSP to). DSP software can read from DSP read FIFO in case *RFIFO_EF* flag is in the '0' state, whereas further writes to DSP read FIFO by host PC software are not allowed while bit D0 of *PCIC_MCSR_RG* register of host PCI-bus interface is in the '1' state (refer to section "Host PCI-bus Interface" later in this chapter and AMCC S5933 PCIC User's Guide for more details).
RFIFO_EF	r	-	Status of the empty flag for DSP read FIFO (PCI-to-DSP FIFO of S5933 PCIC). *RFIFO_EF* =0 indicates that DSP read FIFO is not empty and there is valid unread data in DSP read FIFO. DSP software can read from DSP read FIFO, whereas host PC software can write to DSP read FIFO while bit D0 of *PCIC_MCSR_RG* register of host PCI-bus interface is in the '0' state (refer to section "Host PCI-bus Interface" later in this chapter and AMCC S5933 PCIC User's Guide for more details). *RFIFO_FF* =1 indicates that DSP read FIFO is empty, i.e. it does not contain valid data transferred from host PCI-bus to DSP. Further reads from DSP read FIFO by DSP software are not allowed, whereas host PC software can write to DSP read FIFO while bit D0 of *PCIC_MCSR_RG* register of host PCI-bus interface is in the '0' state (refer to section "Host PCI-bus Interface" later in this chapter and AMCC S5933 PCIC User's Guide for more details)

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

CAUTION

Although the *DSP_FIFO_STAT_RG* IOX register contains status flags for S5933 PCIC FIFO, which are also available via bits #0..#5 of *DSP_PCIC_AGCSTS_RG* S5933 PCIC AOB operation register, it is recommended to use *DSP_FIFO_STAT_RG* IOX register instead of *DSP_PCIC_AGCSTS_RG* S5933 PCIC AOB operation register for run-time monitoring of S5933 PCIC FIFO status.

DSP_FIFO_STAT_RG IOX register is accessed without extra delays, which are applicable when accessing S5933 PCIC AOB operation registers from the DSP environment.

DSP_AMWREN_RG IOX register

DSP_AMWREN_RG read/write IOX register must be used to enable PCI-bus mastering from DSP environment. Table 2-7 provides details about *DSP_AMWREN_RG* IOX register bits.

DSP_AMWREN_RG IOX register (r/w)
(TORNADO-P62xx/P67)

X	X	x	X	x	AM_EN (r)	0	AMR_EN (r/w, 0+)	AMW_EN (r/w, 0+)
bit-31...bit-8	Bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

DSP_AMWREN_RG IOX register (r/w)
(TORNADO-P64xx)

X	0	0	0	0	AM_EN (r)	0	AMR_EN (r/w, 0+)	AMW_EN (r/w, 0+)
bit-31...bit-8	Bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-7. Register bits of *DSP_AMWREN_RG* IOX register.

register bits	access mode	value on DSP reset	Description
AM_EN	r	-	General enable status for PCI-bus mastering from DSP environment. *AM_EN* bit is the read-only copy of *AM_EN* bit of *HIF_CONTROL_RG* HIF register from host PCI-bus interface. *AM_EN* =0 indicates that PCI-bus mastering feature from DSP environment has been disabled by host PC software. DSP software will be unable to initialize PCI-bus mastering via bits *AMW_EN* and *AMR_EN*. In case already active, the PCI-bus mastering will be pending until re-enabled by host PC software. *AM_EN* =1 indicates that PCI-bus mastering that PCI-bus mastering feature from DSP environment has been enabled by host PC software. DSP software can initialize PCI-bus mastering via bits *AMW_EN* and *AMR_EN*.
AMW_EN	r/w	0	Enable control for PCI-bus mastering from DSP environment using DSP-to-PCI data transfers via S5933 PCIC DSP write FIFO (DSP-to-PCI FIFO). *AMW_EN* =0 disables PCI-bus mastering from DSP environment using DSP-to-PCI data transfers via S5933 PCIC DSP write FIFO. *AMW_EN* =1 enables PCI-bus mastering from DSP environment using DSP-to-PCI data transfers via S5933 PCIC DSP write FIFO in accordance with the contents of *DSP_PCIC_MWAR_RG* and *DSP_PCIC_MWTC_RG* AOB operation registers of S5933 PCIC. DSP software can set *AMW_EN* bit to the '1' state only in case *AM_EN* read-only bit is in the '1' state.
AMR_EN	r/w	0	Enable control for PCI-bus mastering from DSP environment using PCI-to-DSP data transfers via S5933 PCIC DSP read FIFO (PCI-to-DSP FIFO). *AMR_EN* =0 disables PCI-bus mastering from DSP environment using PCI-to-DSP data transfers via S5933 PCIC DSP read FIFO. *AMR_EN* =1 enables PCI-bus mastering from DSP environment using PCI-to-DSP data transfers via S5933 PCIC DSP read FIFO in accordance with the contents of *DSP_PCIC_MRAR_RG* and *DSP_PCIC_MRTC_RG* AOB operation registers of S5933 PCIC. DSP software can set *AMR_EN* bit to the '1' state only in case *AM_EN* read-only bit is in the '1' state.

Note:
1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on DSP reset condition.

CAUTION

Bit *AM_EN* can be set by host software via *HIF_CONTROL_RG* (refer to section "Host PCI-bus Interface" later in this chapter), and is used for security purposes in order to prevent unauthorized access and/or destroy of host PC environment from the DSP in case of any malfunction or software failure conditions.

Bit *AM_EN* performs logical AND with bits *AMR_EN* and *AMW_EN* of *DSP_AMWREN_RG* IOX register, and in case bit *AM_EN* is set to logical '0', then bits *AMR_EN* and *AMW_EN* will be both reset to logical '0' state, so DSP will be unable to activate PCI-bus mastering feature.

Refer to the corresponding subsection below for more information about how to program PCI-bus mastering transfers between host PCI-bus environment and the DSP environment.

DSP_XIO_FMT_RG IOX register

DSP_XIO_FMT_RG read/write IOX register is available for *TORNADO-P64xx* DSP systems only and must be used to define data access format to AOB operation registers of on-board AMCC S5933 PCIC and to on-board PIOX/PIOX-16 DCM site interface. Table 2-8 provides details about *DSP_AMWREN_RG* IOX register bits.

DSP_XIO_FMT_RG IOX register (r/w)
(TORNADO-P64xx)

X	*0*	*0*	*0*	*0*	*0*	*PCIC_FMT (r/w, 1+)*	*PX_FMT-1 (r/w, 0+)*	*PX_FMT-0 (r/w, 0+)*
bit-31...bit-8	Bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-8. Register bits of *DSP_XIO_FMT_RG* IOX register for *TORNADO-P64xx*.

register bits	access mode	value on DSP reset	Description
{*PX_FMT-1, PX_FMT-0*}	r/w	[0,0]	Data format selector for access to PIOX/PIOX-16 DCM site interface for *TORNADO-P64xx* DSP systems. {*PX_FMT-1, PX_FMT-0*} =[0,0] selects 8-bit and 16-bit data access formats to PIOX/PIOX-16 DCM data. This setting is a recommended selection for accessing 32-bit PIOX DCM data as 8-bit and/or 16-bit datawords and for access to 16-bit PIOX-16 DCM data as 16-bit dataword (16-bit LSW only of 32-bit dataword). This setting is not allowed for access to 16-bit PIOX-16 DCM data as 32-bit datawords and is not recommended for access to 32-bit PIOX DCM data as 32-bit datawords. {*PX_FMT-1, PX_FMT-0*} =[0,1] selects 32-bit data access format to PIOX/PIOX-16 DCM data. This setting is a recommended selection for access to 32-bit PIOX DCM data as 32-bit datawords. {*PX_FMT-1, PX_FMT-0*} =[1,0] selects 8-bit and 16-bit data access formats to 16-bit LSW of PIOX/PIOX-16 DCM data. This setting is not allowed for access to 32-bit PIOX DCM data, whereas it is a recommended selection for accessing 16-bit PIOX-16 DCM data as either 16-bit or 32-bit datawords.
PCIC_FMT	r/w	1	Data format selector for access to AOB operation registers of AMCC S5933 PCIC for *TORNADO-P64xx* DSP systems. *PCIC_FMT* =0 selects PCIC 8-bit and 16-bit data access formats. This setting is a recommended selection for accessing 32-bit PCIC AOB data as 8-bit and/or 16-bit datawords. *PCIC_FMT* =1 selects PCIC 32-bit data access format. This setting is a recommended selection for accessing 32-bit PCIC AOB data as true 32-bit datawords.

Note:
1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on DSP reset condition.

Refer to the corresponding subsections below for more details about selection of data formats for access to AOB operation registers of AMCC S5933 PCIC and to PIOX/PIOX-16 DCM site interface of *TORNADO-P64xx* DSP systems.

Selection of data format for access to PIOX/PIOX-16 DCM site of TORNADO-P64xx DSP systems

For *TORNADO-P64xx* DSP systems, on-board TMS320C64xx DSP is connected to 16-/32-bit parallel interface of on-board PIOX/PIOX-16 DCM site via TMS320C64xx DSP external 16-bit EMIF-B data bus.

For *TORNADO-P64xx* DSP systems, data access format for accessing PIOX/PIOX-16 DCM site interface from on-board TMS320C64xx DSP is defined via {*PX_FMT-1,PX_FMT-0*} bits of *DSP_XIO_FMT_RG* IOX register (refer to table 2-1b and table 2-8).

CAUTION

Information provided in this subsection is not applicable for *TORNADO-P62xx/P67* DSP systems, which do not provide *DSP_XIO_FMT_RG* IOX register.

TORNADO-P62xx/P67 on-board PIOX/PIOX-16 DCM site interface is connected to on-board TMS320C620x/C6701 DSP via external 32-bit DSP EMIF data bus and data access format is defined directly by the type of DSP external I/O access cycle (8-/16-/32-bit cycle), which is automatically handled by TI C6000 C/Assembler compiler tools via the type of variable used to access PCIC AOB operation registers.

In case {*PX_FMT-1,PX_FMT-0*} bits of *DSP_XIO_FMT_RG* IOX register are set to the [0,0] state, then PIOX/PIOX-16 DCM site interface data can be accessed using 8-bit and 16-bit data access cycles only depending upon the TMS320C64xx external I/O access cycle, which is defined by the type of variable used to access PIOX/PIOX-16 DCM site interface. This setting is set as default on DSP reset condition and is a recommended selection in case either PIOX DCM data shall be accessed as 8-bit and/or 16-bit variables, or in case PIOX-16 DCM data shall be accessed as 16-bit datawords. However, in case 32-bit PIOX DCM data will be accessed as 32-bit variable while {*PX_FMT-1,PX_FMT-0*} bits of *DSP_XIO_FMT_RG* IOX register are set to the [0,0] state, then this will result in splitting 32-bit PIOX access cycle into two 16-bit access cycles (first cycle will access 16-bit LSW and second cycle will access MSW of 32-bit PIOX DCM data) and may result in false synchronization with operation of PIOX DCM hardware.

CAUTION

In case 16-bit PIOX-16 DCM data will be accessed as 32-bit variable while {*PX_FMT-1,PX_FMT-0*} bits of *DSP_XIO_FMT_RG* IOX register are set to the [0,0] state, then this will result in double access to 16-bit PIOX-16 DCM data due to the split of 32-bit access cycle into two 16-bit access cycles (first cycle will access 16-bit LSW and second cycle will access MSW of 32-bit PIOX DCM data). This may deliver false synchronization with PIOX-16 DCM hardware during read cycles and will result in incorrect overwrite of PIOX-16 data during write cycles.

Although setting of {*PX_FMT-1,PX_FMT-0*} bits of *DSP_XIO_FMT_RG* IOX register into the [0,0] state is a universal selection for accessing both PIOX and PIOX-16 DCM data, it is not a recommended selection for accessing 32-bit PIOX DCM data and is not allowed for accessing 16-bit PIOX-16 DCM data as 32-bit variables.

In case {*PX_FMT-1,PX_FMT-0*} bits of *DSP_XIO_FMT_RG* IOX register are set to the [0,1] state, then PIOX/PIOX-16 DCM site interface data can be accessed using 32-bit data access cycles only. This setting is a recommended selection for accessing 32-bit PIOX DCM data as 32-bit datawords, however it will deliver one extra false TMS320C64xx DSP EMIF-B access cycle and will generally reduce overall DSP performance.

Setting of {*PX_FMT-1,PX_FMT-0*} bits of *DSP_XIO_FMT_RG* IOX register to the [1,0] state is generally equivalent to [0,0] setting, however in this case 16-bit MSW of 32-bit PIOX DCM dataword will be never accessed. This setting is a recommended selection for accessing 16-bit PIOX-16 DCM data as either 16-bit or 32-bit datawords with the 16-bit MSW being ignored. However, in case 16-bit PIOX-16 DCM data are accessed

as 32-bit datawords, then this will deliver one extra false TMS320C64xx DSP EMIF-B access cycle and will generally reduce overall DSP performance.

Setting of {*PX_FMT-1,PX_FMT-0*} bits of *DSP_XIO_FMT_RG* IOX register to the [1,1] state is reserved and must not be used by TMS320C64xx DSP application for *TORNADO-P64xx* DSP systems.

Selection of data format for access to AMCC S5933 PCIC AOB operation registers of TORNADO-P64xx DSP systems

For *TORNADO-P64xx* DSP systems, on-board TMS320C64xx DSP is connected to 32-bit AOB operation registers I/O port of on-board AMCC S5933 PCIC via TMS320C64xx DSP external 16-bit EMIF-B data bus.

For *TORNADO-P64xx* DSP systems, data access format for accessing AOB operation registers of on-board AMCC S5933 PCIC from on-board TMS320C64xx DSP is defined via *PCIC_FMT* bit of *DSP_XIO_FMT_RG* IOX register (refer to table 2-1b and table 2-8).

CAUTION

Information provided in this subsection is not applicable for *TORNADO-P62xx/P67* DSP systems, which do not provide *DSP_XIO_FMT_RG* IOX register.

TORNADO-P62xx/P67 on-board AMCC S5933 PCIC is connected to on-board TMS320C620x/C6701 DSP via external 32-bit DSP EMIF data bus and data access format is defined directly by the type of DSP external I/O access cycle (8-/16-/32-bit cycle), which is automatically handled by TI C6000 C/Assembler compiler tools via the type of variable used to access PCIC AOB operation registers.

In case *PCIC_FMT* bit of *DSP_XIO_FMT_RG* IOX register is set to the '0' state, then AOB operation registers of AMCC S5933 PCIC can be accessed using 8-bit and 16-bit data access cycles only depending upon the TMS320C64xx external I/O access cycle, which is defined by the type of variable used to access PCIC AOB registers from DSP application. This setting is recommended for accessing particular bytes and 16-bit halfwords of 32-bit PCIC datawords and is not a recommended setting for accessing full 32-bit PCIC datawords, since all accesses to PCIC AOB registers as 32-bit datawords will be automatically splitted into two 16-bit access cycles (first cycle will access 16-bit LSW and second cycle will access MSW of 32-bit PCIC AOB registers). Note, that when accessing 32-bit PCIC registers using two 16-bit LSW/MSW cycles, then this may provide an error for reading/writing to PCIC AOB incoming/outgoing mailboxes since host PC software may read/write to the corresponding mailbox register between LSW/MSW PCIC access cycles at the DSP side.

In case *PCIC_FMT* bit of *DSP_XIO_FMT_RG* IOX register is set to the '1' state, then AOB operation registers of AMCC S5933 PCIC can be accessed using 8-bit and 32-bit data access cycles depending upon the TMS320C64xx external I/O access cycle, which is defined by the type of variable used to access PCIC AOB registers from DSP application. This setting is set as default on DSP reset condition and is a recommended setting for access to PCIC AOB operation registers, which are typically accessed as 32-bit datawords by most DSP applications. Thus, in case DSP application needs to access particular bytes of 32-bit PCIC AOB datawords while *PCIC_FMT* bit of *DSP_XIO_FMT_RG* IOX register is being set to the '1' state, then these bytes will be accessed directly. However, in case DSP application needs to access PCIC AOB registers as 32-bit datawords,

then those will be accessed as true 32-bit datawords without splitting of PCIC AOB access cycle into two 16-bit LSW/MSW data access cycles.

CAUTION

In case *PCIC_FMT* bit of *DSP_XIO_FMT_RG* IOX register is set to the '1' state, then DSP application cannot access particular 16-bit LSW/MSW of 32-bit PCIC AOB registers.

In case DSP application needs to access particular 16-bit LSW/MSW of 32-bit PCIC AOB registers, then *PCIC_FMT* bit of *DSP_XIO_FMT_RG* IOX register must be set to the '0' state.

CAUTION

In case DSP application accesses *DSP_PCIC_FIFO_RG* AOB operation register of AMCC S5933 PCIC, then this register is accessed as 32-bit dataword disregarding the state of *PCIC_FMT* bit of *DSP_XIO_FMT_RG* IOX register.

It is strongly recommended that DSP application for *TORNADO-P64xx* DSP systems will always accesses *DSP_PCIC_FIFO_RG* AOB operation register of AMCC S5933 PCIC as 32-bit dataword in order to provide PCIC FIFO data integrity. If byte analysis is required for *DSP_PCIC_FIFO_RG* AOB operation register of AMCC S5933 PCIC, then this must be done after 32-bit read or before 32-bit write from/to this register.

DSP_SYS_STAT_RG IOX register

DSP_SYS_STAT_RG IOX register must be used by DSP software in order to get current system configuration for *TORNADO-P6x* DSP systems, to identify *TORNADO-P62/P67* DSP systems, to select external DSP memory (either SBSRAM or SDRAM), which is connected to EMIF CE-2 and CE-3 external memory areas of TMS320C6202/TMS320C6203 DSP for *TORNADO-P6202/P6203* DSP systems only, to identify enabled external interface of TMS320C64xx DSP (either UTOPIA or McBSP1) for *TORNADO-P64xx* DSP systems, and to identify DSP bootmode (either '*NO BOOT*', or '*HPI BOOT*' or '*FLASH BOOT*') for TMS320C64xx DSP of *TORNADO-P64xx* DSP systems.

DSP_SYS_STAT_RG IOX register appears as read-only register for *TORNADO-P62/P67/P64xx* DSP systems and read/write register for *TORNADO-P6202/P6203* DSP systems.

DSP_SYS_STAT_RG IOX register(r/w)
(*TORNADO-P62xx/P67*)

bit-31...bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
x	*x*	*x*	*x*	*x*	*HOST_MODE (r)*	*0 (TORNADO-P62/P67)* *XMEM (r/w,0+) (TORNADO-P6202/P6203)*	*0 (TORNADO-P62/P67)* *1 (TORNADO-P6202/P6203)*	*PCI_ON (r)*

DSP_SYS_STAT_RG IOX register (read-only)
(*TORNADO-P64xx*)

bit-31...bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	Bit-2	bit-1	bit-0
x	*UTOPIA_EN (r)*	*0*	*DSP_BMODE-1 (r)*	*DSP_BMODE-0 (r)*	*HOST_MODE (r)*	*0*	*1*	*PCI_ON (r)*

Table 2-9 provides details about *DSP_SYS_STAT_RG* IOX register bits.

Table 2-9. Register bits of *DSP_SYS_STAT_RG* IOX register.

register bits	access mode	value on DSP reset	Description
PCI_ON	r	-	Indicates whether *TORNADO-P6x* DSP system is installed into PCI-bus slot of host PC. *PCI_ON* =0 indicates that *TORNADO-P6x* DSP system is not installed into PCI-bus slot of host PC and is running in stand-alone mode from external power supply. All DSP accesses to S5933 PCIC will be ignored and read data will be undefined. *PCI_ON* =1 indicates that *TORNADO-P6x* DSP system is installed into PCI-bus slot of host PC. DSP can access PCIC registers and initialize PCI-bus mastering feature.
HOST_MODE	r	-	Indicates whether *TORNADO-P6x* on-board DSP is running either in stand-alone mode or host mode. *HOST_MODE* =0 indicates that *TORNADO-P6x* on-board DSP is running in stand-alone mode, i.e. the reset input of on-board TMS320C6x DSP is not controlled by host PCI-bus interface via *M_GO* bit of *HIF_CONTROL_RG* from host PCI-bus interface. Stand-alone mode assumes that host PCI-bus interface has no control over DSP reset input, which is true in case either *TORNADO-P6x* is removed from PCI-bus slot and is running from external power supply, or *TORNADO-P6x* is installed into host PCI-bus slot and the *M_SA_MODE* bit of *HIF_CONTROL_RG* register of host PCI-bus interface is set to logical '1'. Refer to the corresponding subsection below and to section "Host PCI-bus Interface" later in this chapter for more details. *HOST_MODE* =1 indicates that *TORNADO-P6x* on-board DSP is running under host PCI-bus control, i.e. the reset input of on-board TMS320C6x DSP is controlled by host PCI-bus interface via *M_GO* bit of *HIF_CONTROL_RG* from host PCI-bus interface. Refer to the corresponding subsection below and to section "Host PCI-bus Interface" later in this chapter for more details.
XMEM *(TORNADO-P6202/P6203)*	r/w	0	Selects external memory type for *TORNADO-P6202/P6203* DSP systems at TMS320C6202/TMS320C6203 DSP EMIF CE-2/CE-3 areas. This bit is not used and always reads as '0' for *TORNADO-P62/P67/P64xx* DSP systems. *XMEM* =0 enables external SBSRAM at TMS320C6202/TMS320C6203 DSP EMIF CE-2 area and disables external SDRAM at DSP EMIF CE-2 and CE-3 areas. DSP on-chip EMIF CE-2/CE-3 control registers have to be configured to run with external SBSRAM (table 2-3). *XMEM* =1 enables external SDRAM at TMS320C6202/TMS320C6203 DSP EMIF CE-2/CE-3 areas and disables external SBSRAM at DSP EMIF CE-2 area. DSP on-chip EMIF CE-2/CE-3 control registers have to be configured to run with external SDRAM (table 2-3).

{*DSP_BMODE-1, DSP_BMODE-0*} (*TORNADO-P64xx*)	r	-	Return DSP bootmode ID for *TORNADO-P64xx* DSP systems. Refer to table 2-2b for more details about DSP bootmode configurations for *TORNADO-P64xx* DSP systems. {*DSP_BMODE-1, DSP_BMODE-0*} =[0,0] denotes that DSP has started in '*NO BOOT*' bootmode. {*DSP_BMODE-1, DSP_BMODE-0*} =[0,1] denotes that DSP has started in '*HPI BOOT*' bootmode. {*DSP_BMODE-1, DSP_BMODE-0*} =[1,0] denotes that DSP has started in '*FLASH BOOT*' bootmode. {*DSP_BMODE-1, DSP_BMODE-0*} =[1,1] is reserved.
UTOPIA_EN (*TORNADO-P6415/P6416*)	r	-	Indicates whether *TORNADO-P6415/P6416* on-board TMS320C6415/C6416 DSP has external either UTOPIA or McBSP1 interface enabled. This bit always reads as '0' for *TORNADO-P6414* DSP systems, which do not support UTOPIA interface. Refer to the corresponding subsections below and to section "Serial I/O Expansion Interface (SIOX)" later in this chapter for more details. *UTOPIA_EN* =0 indicates that *TORNADO-P6415/P6416* on-board DSP has UTOPIA interface disabled and McBSP1 serial port enabled. *UTOPIA_EN* =1 indicates that *TORNADO-P6415/P6416* on-board DSP has UTOPIA interface enabled and McBSP1 serial port disabled.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on DSP reset condition.

Read-only bit D1 of ***DSP_SYS_STAT_RG*** register is used for identification of ***TORNADO-P6x*** DSP systems as described in table 2-13. This bit always reads as '0' for ***TORNADO-P62/P67*** DSP systems, which do not provide ***DSP_DEV_ID_RG*** IOX register, whereas it reads as '1' for ***TORNADO-P6202/P6203/P64xx*** DSP systems, which provide ***DSP_DEV_ID_RG*** IOX register. Refer to table 2-13 and the corresponding subsection below for more details.

Watchdog Timer (WDT) control

TORNADO-P6x DSP systems provide on-board watchdog timer (WDT), which can be used to increase DSP software operation reliability for both DSP stand-alone and host PC operation modes.

WDT is an on-board hardware timer, which sets its output WDT expiration event in case WDT has not been reset within approximately 0.8 sec after last WDT reset. In case WDT is being reset periodically by DSP software with the period less than 0.8 sec, then WDT output expiration event will never be set. Note, that it is completely up to the user whether to use on not to use WDT feature of ***TORNADO-P6x*** DSP system.

TORNADO-P6x DSP systems support generation of DSP reset signal on WDT expiration event for DSP stand-alone operation mode only (refer to subsection "TMS320C6x DSP operation modes and reset control" earlier in this section), and generation of DSP external interrupt on WDT expiration event for both DSP stand-alone and host PC operation mode. Particular configuration is set by DSP application via the corresponding IOX registers.

Generation of DSP reset signal on WDT expiration event is the most radical solution and will result in DSP hardware reset and application restart on WDT expiration event. Thus, in case this feature is enabled for DSP stand-alone operation mode and DSP software is operating normally, then it must periodically reset WDT by means of writing to the *DSP_WDT_CLR_RG* IOX register with the period less than 0.8 sec in order to exclude WDT expiration. However, in case DSP software will either idle or hangs on during more than 0.8 sec, then DSP hardware reset will apply and DSP application will restart.

Generation of DSP external interrupt on WDT expiration event is the 'smooth' and flexible solution in order to perform restart of either all DSP application or its specific part only on WDT expiration event. Most typically, TMS320C6x external non-maskable interrupt (NMI) is being used to interrupt DSP on WDT expiration event, since it is not effected by interrupt masks. Note, that generation of DSP external interrupt on WDT expiration event is applicable for both DSP stand-alone and host PC operation modes. When operating normally, DSP application must periodically reset WDT by means of writing to the *DSP_WDT_CLR_RG* IOX register with the period less than 0.8 sec in order to exclude WDT expiration. However, in case DSP software will either idle or hangs on during more than 0.8 sec, then selected DSP external interrupt (typically NMI) will apply, which can restart either all DSP software or its specific part(s).

Generation of DSP reset signal on active WDT event is available for DSP stand-alone mode only and is enabled by the *WDT_EN* bit of *DSP_WDT_EN_RG* IOX register.

DSP_WDT_EN_RG IOX register (r/w)
(*TORNADO-P62xx/P67*)

X	*x*	*x*	*x*	*x*	*0*	*0*	*0*	*WDT_EN (r/w, 0+)*
bit-31...bit-8	bit-7	bit-6	bit-5	Bit-4	bit-3	bit-2	bit-1	bit-0

DSP_WDT_EN_RG IOX register (r/w)
(*TORNADO-P64xx*)

X	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*WDT_EN (r/w, 0+)*
bit-31...bit-8	bit-7	bit-6	bit-5	Bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-10 provides details about *DSP_WDT_EN_RG* IOX register bits.

Table 2-10. Register bits of *DSP_WDT_EN_RG* register.

register bits	access mode	value on DSP reset	Description
WDT_EN	R/w	0	Enable control for generation of DSP reset signal on WDT expiration event for DSP stand-alone operation. *WDT_EN* =0 disables generation of DSP reset signal on WDT expiration event during DSP stand-alone operation. *WDT_EN* =1 enable generation of DSP reset signal on WDT expiration event during DSP stand-alone operation. DSP software must periodically reset WDT (once within 0.8 sec) by means of writing to the *DSP_WDT_CLR_RG* register (written data is ignored) in order to exclude automatic DSP restart.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on DSP reset condition.

CAUTION

In case DSP application requires to generate DSP interrupt on WDT expiration event in either DSP stand-alone or host PC mode, then DSP software must load 0BH value to the corresponding *DSP_EXT_INT4_SEL_RG…DSP_EXT_INT7_SEL_RG* or *DSP_NMI_SEL_RG* IOX register (refer to the corresponding subsection below for more details).

CAUTION

In case either DSP operation mode is set with WDT enabled, or any of DSP external interrupt selectors is configured to generate interrupt on WDT expiration event, then DSP software must periodically reset WDT by writing to the *DSP_WDT_CLR_RG* IOX register (refer to table 2-1). Data written to the *DSP_WDT_CLR_RG* IOX register is ignored.

The time interval between succeeding WDT resets must not exceed 0.8 sec, otherwise WDT expiration event will apply.

DSP_WDT_CLR_RG IOX register (write-only)

x	x	x	X	X	x	x	x	x
bit-31...bit-8	bit-7	bit-6	bit-5	bit-4	Bit-3	bit-2	bit-1	bit-0

Reset control for SIOX/PIOX DCM sites via DSP_PXSX_RESET_RG IOX register

TORNADO-P6x provide software programmable individual reset signals for each SIOX and PIOX/PIOX-16 DCM sites (refer to the corresponding sections later in this chapter). Since SIOX and PIOX/PIOX-16 DCM are designed to be reset by the corresponding SIOX and PIOX/PIOX-16 DCM reset signal, then this allows correct initialization of installed SIOX and PIOX/PIOX-16 DCM hardware and synchronization with *TORNADO-P6x* DSP software.

The reset signals for SIOX and PIOX/PIOX-16 DCM sites are controlled by DSP software via *DSP_PXSX_RESET_RG* IOX register (refer to table 2-1).

DSP_PXSX_RESET_RG IOX register (r/w)
(*TORNADO-P62xx/P67*)

X	x	x	x	x	0	$\overline{SXB\_RESET}$ (r/w, 0+)	$\overline{SXA\_RESET}$ (r/w, 0+)	$\overline{PX\_RESET}$ (r/w, 0+)
bit-31...bit-8	bit-7	bit-6	bit-5	bit-4	Bit-3	bit-2	bit-1	bit-0

DSP_PXSX_RESET_RG IOX register (r/w)
(*TORNADO-P64xx*)

X	0	0	0	0	0	$\overline{SXB\_RESET}$ (r/w, 0+)	$\overline{SXA\_RESET}$ (r/w, 0+)	$\overline{PX\_RESET}$ (r/w, 0+)
bit-31...bit-8	bit-7	bit-6	bit-5	bit-4	Bit-3	bit-2	bit-1	bit-0

Table 2-11 provides details about *DSP_PXSX_RESET_RG* IOX register bits.

Table 2-11. Register bits of *DSP_PXSX_RESET_RG* register.

register bits	access mode	value on DSP reset	Description
$\overline{PX\_RESET}$	r/w	0	Reset control for PIOX/PIOX-16 DCM site. Refer to section "Parallel I/O Expansion DCM site (PIOX/PIOX-16)" later in this chapter for more details. *PX_RESET* =0 sets active reset signal for PIOX/PIOX-16 DCM site and installed PIOX/PIOX-16 DCM hardware. *PX_RESET* =1 removes reset signal for PIOX/PIOX-16 DCM site and enables operation of installed PIOX/PIOX-16 DCM hardware.
$\overline{SXA\_RESET}$	r/w	0	Reset control for SIOX-A rev.B site and SIOX-A rev.C DCM site. Refer to section "Serial I/O Expansion DCM Sites (SIOX)" later in this chapter for more details. *SXA_RESET* =0 sets active reset signal for SIOX-A rev.B and SIOX-A rev.C DCM sites and installed SIOX DCM hardware. *SXA_RESET* =1 removes reset signal for SIOX-A rev.B and SIOX-A rev.C DCM sites and enables operation of installed SIOX DCM hardware.
$\overline{SXB\_RESET}$	r/w	0	Reset control for SIOX-B rev.C DCM site. Refer to section "Serial I/O Expansion DCM Sites (SIOX)" later in this chapter for more details. *SXB_RESET* =0 sets active reset signal for SIOX-B rev.C DCM site and installed SIOX DCM hardware. *SXB_RESET* =1 removes reset signal for SIOX-B rev.C DCM site and enables operation of installed SIOX DCM hardware.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on DSP reset condition.

DSP_HM_RQ0_RG and DSP_HM_RQ1_RG IOX registers for reception of interrupt request from host PCI-bus

DSP_HM_RQ0_RG and *DSP_HM_RQ1_RG* IOX registers are read-only registers, which can be used for communication between host PCI-bus and DSP environment via PCI-to-DSP interrupt generation and 4-bit passed token (bits D3..D0):

DSP_HM_RQ0_RG IOX register (read-only, cleared on writes)
DSP_HM_RQ1_RG IOX register (read-only, cleared on writes)
(*TORNADO-P62xx/P67*)

X	*X*	*X*	*X*	*x*	*D3* *(r)*	*D2* *(r)*	*D1* *(r)*	*D0* *(r)*
bit-31...bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

DSP_HM_RQ0_RG IOX register (read-only, cleared on writes)
DSP_HM_RQ1_RG IOX register (read-only, cleared on writes)
(*TORNADO-P64xx*)

X	*0*	*0*	*0*	*0*	*D3 (r)*	*D2 (r)*	*D1 (r)*	*D0 (r)*
bit-31...bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

The *DSP_HM_RQ0_RG* and *DSP_HM_RQ1_RG* IOX registers are actually the read-only contents of *HIF_HM_RQ0_RG* and *HIF_HM_RQ1_RG* read/write registers of host PCI-bus interface (refer to section "Host PCI-bus Interface" later in this chapter).

When host PCI-bus writes to *HIF_HM_RQ0_RG* register, then this event can generate active *HM_RQ0* PCI-to-DSP interrupt in case any of DSP external interrupt selector registers is configured for DSP interrupt on *HM_RQ0* event (refer to subsection "DSP External Interrupt Selectors" later in this section). Similarly, when host PCI-bus writes to *HIF_HM_RQ1_RG* register, then this event can generate active *HM_RQ1* PCI-to-DSP interrupt in case another of DSP external interrupt selector register is configured for DSP interrupt on the *HM_RQ1* event.

The 4-bit token, which is passed via *DSP_HM_RQ0_RG* and *DSP_HM_RQ1_RG* IOX registers from host PCI-bus master to DSP, might be used by the DSP software to identify the interrupt specific information. After DSP has read and decoded the contents of *DSP_HM_RQ0_RG* and *DSP_HM_RQ1_RG* IOX registers, it can clear the contents of these registers in order to confirm host PCI-bus master that the request has been processed (the requesting host PCI-bus master might perform periodical polling of the contents of the *HIF_HM_RQ0_RG* and *HIF_HM_RQ1_RG* read/write registers in order to ensure that request has been processed by DSP).

CAUTION

DSP can reset the contents of *DSP_HM_RQ0_RG* and *DSP_HM_RQ1_RG* IOX registers by means of writing to these registers in accordance with table 2-1. Data written is being ignored and the contents of the addressed register is being cleared on the write condition.

The *DSP_HM_RQ0_RG* and *DSP_HM_RQ1_RG* IOX registers operate as 4-bit incoming mailbox registers between the host PCI-bus and DSP environment, and are similar to 32-bit incoming mailbox registers *DSP_PCIC_IMBXx_RG*, which are the part of the S5933 PCIC. However, despite the S5933 PCIC incoming mailboxes, DSP can clear the contents of *DSP_HM_RQ0_RG* and *DSP_HM_RQ1_RG* IOX registers after the request has been processed and each of these registers can generate an individual interrupt request to the DSP. The latter feature adds two independent interrupt channels into PCI-to-DSP interrupt communication along with the *DSP_DPRAM_IRQ* interrupt from DPRAM and the AOB interrupt from AMCC S5933 PCIC, and allows two external PCI-bus masters to generate two independent PCI-to-DSP interrupts for *TORNADO-P6x* on-board DSP, so simplifying the DSP decoding software and reducing the interrupt processing times.

DSP_MH_RQ_RG IOX register for generation interrupt request to host PCI-bus

DSP_MH_RQ_RG is the write only IOX registers, which is used for generation *MH_RQ* interrupt from DSP to the PCI environment. Data written is ignored. Refer to section "Host PCI-bus Interface" for more details about PCI-bus interrupt generation.

DSP_MH_RQ_RG IOX register (write-only)

X	x	x	x	x	x	x	x	x
bit-31...bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

DSP external interrupt selectors

TORNADO-P6x DSP systems provide DSP software configured selectors for each of the DSP external interrupts (EXT_INT4..EXT_INT7, NMI). Since the number of available external DSP interrupt sources is well above five sources for *TORNADO-P6x* DSP systems, then this allows outstanding flexibility for run-time configuration of DSP external interrupt source selectors in order to meet requirements of any DSP application.

Selection of particular interrupt source for DSP external interrupts (EXT_INT4..EXT_INT7, NMI) is performed by the DSP software by means of programming the *DSP_EXT_INT4_SEL_RG.. DSP_EXT_INT7_SEL_RG* and *DSP_NMI_SEL_RG* IOX registers (table 2-1):

DSP_EXT_INT4_SEL_RG IOX register (r/w)
DSP_EXT_INT5_SEL_RG IOX register (r/w)
DSP_EXT_INT6_SEL_RG IOX register (r/w)
DSP_EXT_INT7_SEL_RG IOX register (r/w)
DSP_NMI_SEL_RG IOX Register (r/w)
(*TORNADO-P62xx/P67*)

x	X	x	x	x	*INT_SEL-3 (r/w, 0+)*	*INT_SEL-2 (r/w, 0+)*	*INT_SEL-1 (r/w, 0+)*	*INT_SEL-0 (r/w, 0+)*
bit-31...bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

DSP_EXT_INT4_SEL_RG IOX register (r/w)
DSP_EXT_INT5_SEL_RG IOX register (r/w)
DSP_EXT_INT6_SEL_RG IOX register (r/w)
DSP_EXT_INT7_SEL_RG IOX register (r/w)
DSP_NMI_SEL_RG IOX Register (r/w)
(*TORNADO-P64xx*)

x	0	0	0	0	*INT_SEL-3 (r/w, 0+)*	*INT_SEL-2 (r/w, 0+)*	*INT_SEL-1 (r/w, 0+)*	*INT_SEL-0 (r/w, 0+)*
bit-31...bit-8	bit-7	Bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

CAUTION

DSP_EXT_INT4_SEL_RG.. DSP_EXT_INT7_SEL_RG interrupt selector registers correspond to programming the interrupt source for EXT_INT4..EXT_INT7 external interrupt inputs of TMS320C6x DSP.

DSP_NMI_SEL_RG interrupt selector register corresponds to programming the interrupt source for external non-maskable interrupt input (NMI) of TMS320C6x DSP.

Each DSP external interrupt selector register of *TORNADO-P6x* allows selection from 11 available interrupt sources for *TORNADO-P62xx/P67* DSP systems and from 14 available interrupt sources for *TORNADO-P64xx* DSP systems in accordance with table 2-12. All DSP external interrupt selector registers default to the 00H state on DSP reset condition, which corresponds to unselected interrupt source (disabled interrupt).

Table 2-12. Interrupt sources for DSP external interrupt selectors.

{INT_SEL-3..INT_SEL-0} bits of DSP_EXT_INT4_SEL_RG DSP_EXT_INT5_SEL_RG DSP_EXT_INT6_SEL_RG DSP_EXT_INT7_SEL_RG DSP_NMI_SEL_RG DSP External Interrupt Source Selector Registers				**DSP Interrupt source**
***INT_SEL-3* bit**	***INT_SEL-2* bit**	***INT_SEL-1* bit**	***INT_SEL-0* bit**	
0	*0*	*0*	*0*	Interrupt is disabled. This is default value on DSP reset condition.
0	*0*	*0*	*1*	External *XIRQ-0* interrupt request from SIOX-A rev.B and SIOX-A rev.C DCM sites of *TORNADO-P62xx/P67* DSP systems. External *PX_IRQ-0* interrupt request from PIOX/PIOX-16 DCM site of *TORNADO-P64xx* DSP systems.
0	*0*	*1*	*0*	External *XIRQ-1* interrupt request from SIOX-A rev.B and SIOX-B rev.C DCM sites of *TORNADO-P62xx/P67* DSP systems. External *PX_IRQ-1* interrupt request from PIOX/PIOX-16 DCM site of *TORNADO-P64xx* DSP systems.
0	*0*	*1*	*1*	External *XIRQ-2* interrupt request from SIOX-A rev.B and PIOX/PIOX-16 DCM sites of *TORNADO-P62xx/P67* DSP systems. External *PX_IRQ-2* interrupt request from PIOX/PIOX-16 DCM site of *TORNADO-P64xx* DSP systems.

0	*1*	*0*	*0*	External *XIRQ-3* interrupt request from PIOX/PIOX-16 DCM site of *TORNADO-P62xx/P67* DSP systems. External *PX_IRQ-3* interrupt request from PIOX/PIOX-16 DCM site of *TORNADO-P64xx* DSP systems.
0	*1*	*0*	*1*	Interrupt request from DPRAM (*DSP_DPRAM_IRQ*) of *TORNADO-P62xx/P67* DSP systems and *TORNADO-P64xx* DSP systems with 256Kx32 DPRAM. Interrupt request will be cleared after DSP reads from *DPRAM_HM_RQ* DPRAM memory location. Reserved for *TORNADO-P64xx* DSP systems with 128Kx32 DPRAM. Interrupt is disabled.
0	*1*	*1*	*0*	*HM_RQ0* interrupt request on the PCI-bus writes to *HIF_HM_RQ0_RG* register event. DSP can read the passed 4-bit token from PCI-bus via *DSP_HM_RQ0_RG* register.
0	*1*	*1*	*1*	*HM_RQ1* interrupt request on the PCI-bus writes to *HIF_HM_RQ1_RG* register event. DSP can read the passed 4-bit token from PCI-bus via *DSP_HM_RQ1_RG* register.
1	*0*	*0*	*0*	AOB interrupt request from S5933 PCIC on mailbox or end of the PCI-bus mastering conditions. Interrupt request must be identified and cleared via *PCIC_DSP_AINT_RG* register of S5933 PCIC.
1	*0*	*0*	*1*	Interrupt request on write-FIFO (DSP-to-PCI FIFO) ready condition (write-FIFO is not full). New interrupt request will be generated after DSP writes to the *PCIC_DSP_FIFO_RG* of S5933 PCIC.
1	*0*	*1*	*0*	Interrupt request on read-FIFO (PCI-to-DSP FIFO) ready condition (read-FIFO is not empty). New interrupt request will be generated after DSP reads from the *PCIC_DSP_FIFO_RG* of S5933 PCIC.
1	*0*	*1*	*1*	Interrupt request on WDT expiration event.
1	*1*	*0*	*0*	Reserved. Interrupt is disabled.
1	*1*	*0*	*1*	Reserved for *TORNADO-P62xx/P67* DSP systems. Interrupt is disabled. External *SX_IRQ-0* interrupt request from SIOX-A rev.B and SIOX-A rev.C DCM sites of *TORNADO-P64xx* DSP systems.
1	*1*	*1*	*0*	Reserved for *TORNADO-P62xx/P67* DSP systems. Interrupt is disabled. External *SX_IRQ-1* interrupt request from SIOX-A rev.B and SIOX-B rev.C DCM sites of *TORNADO-P64xx* DSP systems.

1	*1*	*1*	*1*	Reserved for *TORNADO-P62xx/P67* DSP systems. Interrupt is disabled. External *SX_IRQ-2* interrupt request from SIOX-A rev.B DCM site of *TORNADO-P64xx* DSP systems.

Note: 1. Highlighted configurations correspond to default settings on DSP reset condition.

CAUTION

EXTERNAL INTERRUPT POLARITY register (@0x019C0008) of TMS320C6x DSP must be set to the 0x00000000 value in order to meet hardware requirements of *TORNADO-P6x* DSP system, which corresponds to active low-to-high interrupt transitions.

Identification of TORNADO-P6x DSP system from DSP software

TORNADO-P6x DSP systems product line comprises of a variety of DSP systems with different on-board DSP type, different DSP performance, different DSP on-chip resources and different on-board hardware resources.

In case TMS320C6x DSP software for *TORNADO-P6x* DSP systems requires to identify particular *TORNADO-P6x* DSP system platform (i.e. on-board DSP chip type) in order to perform *TORNADO-P6x* platform specific operations (this typically include initialization of DSP EMIF control registers, DSP on-chip HPI port control, DSP on-chip floating-point operations control, DSP on-chip timer configuration, DSP on-chip McBSP control, etc.), then this can be done using the following *TORNADO-P6x* on-board and DSP on-chip resources:

- D1 bit of *DSP_SYS_STAT_RG* IOX register (refer to the corresponding subsection above)
- {*DEV_ID-3..DEV_ID-0*} bit field of *DSP_DEV_ID_RG* IOX register (*TORNADO-P6202/P6203* DSP systems only)
- *CPU_ID* bit field of TMS320C6x DSP on-chip CSR register (refer to original TI TMS320C6x documentation for more details).
- {*REV_ID-3..REV_ID-0*} bit field of *DSP_DEV_ID_RG* IOX register (*TORNADO-P64xx* DSP systems only).

CAUTION

TORNADO-P6x on-board TMS320C6x DSP environment does not provide resources for identification of installed DPRAM, SBSRAM and SDRAM capacity.

In case *TORNADO-P6x* DSP system is installed into PCI-bus slot of host PC, then both DSP software and/or host PC software can read DPRAM/SBSRAM/SDRAM configuration information for *TORNADO-P6x* DSP system from host PCI-bus interface.

In case *TORNADO-P6x* DSP system is not installed into PCI-bus slot of host PC, then DSP software must apply appropriate software technique in order to determine on-board DPRAM/SBSRAM/SDRAM configuration.

DSP_DEV_ID_RG read-only IOX register is available for *TORNADO-P6202/P6203/P64xx* DSP systems and includes {*DEV_ID-3..DEV_ID-0*} device identification code, which is used to identify particular *TORNADO-P6x* DSP system except for *TORNADO-P62/P67* DSP systems.

DSP_DEV_ID_RG IOX register (read-only)
(*TORNADO-P6202/P6203*)

X	*x*	*x*	*x*	*X*	*DEV_ID-3 (r)*	*DEV_ID-2 (r)*	*DEV_ID-1 (r)*	*DEV_ID-0 (r)*
Bit-31...bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

DSP_DEV_ID_RG IOX register (read-only)
(*TORNADO-P64xx*)

X	*REV_ID-3 (r)*	*REV_ID-2 (r)*	*REV_ID-1 (r)*	*REV_ID-0 (r)*	*DEV_ID-3 (r)*	*DEV_ID-2 (r)*	*DEV_ID-1 (r)*	*DEV_ID-0 (r)*
Bit-31...bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Identification of *TORNADO-P6x* DSP system (table 2-13) must begin with the read-only D1 bit of *DSP_SYS_STAT_RG* register (refer to table 2-9 and the corresponding subsection earlier in this section), which indicates availability of *DSP_DEV_ID_RG* extended device ID register for *TORNADO-P6x* DSP systems. Bit D1 of *DSP_SYS_STAT_RG* register reads as '0' for *TORNADO-P62/P67* DSP systems and as '1' for *TORNADO-P6202/P6203/P64xx* DSP systems.

Further identification between *TORNADO-P62* and *TORNADO-P67* DSP systems must be done by DSP software via *CPU_ID* bit field of TMS320C6x DSP on-chip CSR register, whereas *TORNADO-P6202/P6203/P64xx* DSP systems shall be identified via {*DEV_ID-3..DEV_ID-0*} bit field of *DSP_DEV_ID_RG* extended device ID IOX register. If required, DSP application can also identify optional silicon revision of TMS320C6x DSP via *REV_ID* bit field of TMS320C6x DSP on-chip CSR register and via DIE_ID on-chip register (at DSP memory address 0x01b00200) of TMS320C64xx DSP (*TORNADO-P64xx* DSP systems only).

Table 2-13. Identification of *TORNADO-P6x* DSP system from DSP environment.

TORNADO **DSP System**	**D1 bit of** ***DSP_SYS_STAT_RG*** **IOX register**	**{*DEV_ID-3..DEV_ID-0*} bits of** ***DSP_DEV_ID_RG*** **IOX register**	***CPU_ID*** **bit field (bits 31..24) of DSP on-chip CSR register**	***REV_ID*** **bit field (bits 23..16) of DSP on-chip CSR register**
TORNADO-P62	0	-	0x00	0x01 0x02
TORNADO-P67	0	-	0x02	0x01 0x02
TORNADO-P6202	1	0x2	0x00	0x02 0x03
TORNADO-P6203	1	0x3	0x00	0x03
TORNADO-P6414	1	0x8	0x0c	0x01
TORNADO-P6415	1	0x9	0x0c	0x01
TORNADO-P6416	1	0xa	0x0c	0x01

Note: 1. *REV_ID* bit field of TMS320C6x DSP on-chip CSR register is optional and can be used to identify revision code of TMS320C6x DSP.

Firmware revision identification for TORNADO-P64xx DSP systems

TORNADO-P64xx DSP systems also provide optional {*REV_ID-3..REV_ID-0*} bit field of *DSP_DEV_ID_RG* IOX register, which can be used to identify revision ID for *TORNADO-P64xx* on-board firmware as the following:

- {*REV_ID-3..REV_ID-0*} =[0,0,0,1] corresponds to initial firmware revision '1A' of *TORNADO-P64xx* DSP system.

TMS320C6x HPI (host port interface)

TORNADO-P6x offers access from host PCI-bus I/O interface to TMS320C6x on-chip 32-bit HPI (host port interface). For details about HPI port of *TORNADO-P6x* DSP systems refer to "Host PCI-bus Interface" section later in this chapter.

TORNADO-P62/P67/P64xx DSP systems provide full support for DSP on-chip HPI port including mutual interrupt generation between host PCI-bus I/O interface and TMS320C6x DSP. *TORNADO-P62/P67* DSP systems offer 16-bit HPI port, whereas *TORNADO-P64xx* DSP systems provide 32-bit HPI port.

TORNADO-P6202/P6203 DSP systems provide support for 32-bit asynchronous host port mode of TMS320C6202/TMS320C6203 DSP on-chip expansion bus, which is similar to TMS320C6201/TMS320C6701 DSP on-chip HPI port. TMS320C6202/TMS320C6203 DSP cannot generate interrupt request to host PCI-bus via HPI port, however host PCI-bus can generate interrupt request to TMS320C6202/TMS320C6203 DSP via HPI port (DSPINT bit of XBHC register).

For details about TMS320C6201/C6701/C64xx DSP on-chip HPI port and TMS320C6202/TMS320C6203 expansion bus refer to original TI documentation for TMS320C6x DSP.

Generation of DSP-to-PCI interrupts

TORNADO-P6x supports several paths for generation interrupt request from DSP environment to host PCI-bus interface (refer to section "Host PCI-bus Interface" for more details):

- *MH_RQ* interrupt request, which is set in case DSP writes to the *DSP_MH_RQ_RG* IOX register (data is ignored). *MH_RQ* interrupt request generates host PCI-bus interrupt request in case *MH_RQ_IE* bit of *HIF_IE_RG* register from host PCI-bus I/O interface is set to the '1' state, and *HOST_PCIC_INTCSR_RG* PCI-bus operation register of AMCC S5933 PCIC is configured to generate host PCI-bus interrupt on the load event of byte #3 of incoming mailbox #4.
- *DPRAM_MH_RQ* interrupt request, which is set in case DSP writes to the *DPRAM_MH_RQ* DPRAM memory location (data is ignored), and *HOST_PCIC_INTCSR_RG* PCI-bus operation register of AMCC S5933 PCIC is programmed to generate PCI-bus interrupt on the incoming mailbox #4 byte #3 load event. *DPRAM_MH_RQ* interrupt request is available for *TORNADO-P62xx/P67* DSP systems and *TORNADO-P64xx* DSP systems with 256Kx32 DPRAM.
- when DSP writes to any of the *DSP_PCIC_OMBX0_RG..DSP_PCIC_OMBX3* registers and in case *HOST_PCIC_INTCSR_RG* PCI-bus operation register of AMCC S5933 PCIC is programmed to generate PCI-bus interrupt on the corresponding input mailbox event.
- when DSP reads from any of the *DSP_PCIC_IMBX0_RG..DSP_PCIC_IMBX3* PCIC register and in case *HOST_PCIC_INTCSR_RG* PCI-bus operation register of AMCC S5933 PCIC is programmed to generate PCI-bus interrupt on the corresponding output mailbox event.
- *HPI_HINT* host interrupt request via TMS320C6x DSP on-chip HPI port (*TORNADO-P62/P67/P64xx* DSP systems only), which is set by DSP software via *HINT* bit of HPIC register (refer to TI TMS320C6x DSP documentation for more details). *HPI_HINT* interrupt request generates active host PCI-bus interrupt request in case *HPI_HINT_IE* bit of *HIF_IE_RG* register from host PCI-bus I/O interface is set to the '1' state, and *HOST_PCIC_INTCSR_RG* PCI-bus operation register of AMCC S5933 PCIC is configured to generate host PCI-bus interrupt on the load event of byte #3 of incoming mailbox #4.

DSP controlled PCI-bus mastering

TORNADO-P6x DSP systems support data transfer between the DSP and PCI-bus environments using DSP controlled PCI-bus mastering feature of AMCC S5933 PCIC.

DSP controlled PCI-bus mastering provides 'transparent visibility' of full PCI-bus memory and I/O address spaces for *TORNADO-P6x* on-board DSP, 'virtually expands' *TORNADO-P6x* on-board RAM and DSP on-chip memory, and allows real-time communication between *TORNADO-P6x* on-board DSP and installed PCI-bus devices (including other *TORNADO* PCI-bus plug-in DSP systems).

CAUTION

TORNADO-P6x DSP systems features PCI-bus mastering, which can be initialized and controlled by on-board TMS320C6x DSP.

Host PC application can enable/disable DSP controlled PCI-bus mastering via *AM_EN* bit of *HIF_CONTROL_RG* HIF register (refer to section "Host PCI-bus Interface" later in this chapter) in order to preserve integrity of host PC environment and to exclude possible unauthorized PCI-bus mastering access from DSP environment when DSP reset signal is released without valid DSP code uploaded.

Host PCI-bus mastering assumes that data transfers between DSP environment and host PCI-bus environment are performed via AMCC S5933 PCIC on-chip read/write FIFO under control of PCIC on-chip programmable DMA controllers. Host PCI-bus mastering feature does not involve any of host PC CPU resources and allows to transfer data between DSP environment and host PCI-bus environment in-parallel with host PC operation. Moreover, in case PCIC FIFO access is handled by DSP on-chip DMA controller, then DSP CPU kernel is also excluded from data transfers between DSP environment and host PCI-bus environment.

The following is example of programming DSP-to-PCI transfers using DSP controlled PCI-bus mastering feature of AMCC S5933 PCIC:

- host PC application defines PCI-bus start address and block length for DSP-to-PCI transfer and transfers these parameters to DSP application either via DPRAM or DSP on-chip HPI port
- host PC application sets *AM_EN* bit of *HIF_CONTROL_RG* HIF register to the '1' state in order to enable DSP controlled host PCI-bus mastering
- host PC application sets synchro-flag to DSP (via DPRAM, DPSEM, etc) in order to notify DSP that host PCI-bus mastering can be initialized
- DSP application checks that the *AM_EN* bit of *HIF_CONTROL_RG* register is set to the '1' state in order to ensure that host PCI-bus mastering is enabled by host PC application
- DSP application sets bits *TRANSFER_COUNT_ENABLE* (bit #28) and *RESET_ADDON_TO_PCI_FIFO_STATUS_FLAGS* (bit #25) of *DSP_PCIC_AGCSTS_RG* register of AMCC S5933 PCIC to the '1' state
- DSP application reads PCI-bus start address and block length parameters, which have been passed by host PC application to DSP application via either on-board DPRAM or DSP on-chip HPI port, and configures *DSP_PCIC_MWAR_RG* and *DSP_PCIC_MWTC_RG* PCIC AOB operation registers of AMCC S5933 PCIC
- DSP application sets *AMW_EN* bit of *DSP_AMWREN_RG* IOX register to the '1' state in order to activate host PCI-bus mastering
- DSP application continuously writes transferred data to *DSP_PCIC_FIFO_RG* PCIC AOB register using either direct write from DSP application DSP on-chip DMA controller until complete data arrays will be transferred.

In order to exclude application specific details, the above example does not show how to load AMCC S5933 PCIC FIFO from DSP application and how to process interrupts on FIFO write condition in DSP application. Below are some general recommendations for how to write data to AMCC S5933 PCIC FIFO and how to process interrupts on FIFO write ready condition in DSP application.

Host PCI-bus mastering feature is typically used to transfer large data-arrays between DSP application and host PC application. Instead, small shared data arrays and shared variables can be directly allocated in high-density

on-board DPRAM, or can be even allocated in DSP on-chip memory, SBSRAM or SDRAM and accessed by host PC application via DSP on-chip HPI port.. The most DSP time saving method to handle FIFO data streams from DSP application is to use TMS320C6x DSP on-chip DMA (or EDMA) controller. The following example shows how to program DSP-to-host data transfers via AMCC S5933 PCIC FIFO using TMS320C620x/C6701 DSP on-chip DMA controller for *TORNADO-P62xx/P67* DSP systems:

- DSP application programs any of *DSP_EXT_INT4_SEL_RG.. DSP_EXT_INT7_SEL_RG* IOX registers in order to configure any of DSP external interrupt to occur on AMCC S5933 PCIC write-FIFO ready condition (the corresponding external DSP interrupt must be disabled via the TMS320C6x DSP on-chip IMR interrupt mask register)
- DSP application configures TMS320C620x/C6701 DSP on-chip *DMA_PRIMARY_CONTROL_REGISTER*, *DMA_SECONDARY_CONTROL_REGISTER*, *DMA_SOURCE_ADDRESS_REGISTER*, *DMA_DESTINATION_ADDRESS_REGISTER* and *DMA_TRANSFER_COUNTER* registers of any of the DSP on-chip DMA controllers to use synchro-event on the corresponding DSP external interrupt input, DSP source address with address autoincrement feature, DSP destination address as *DSP_PCIC_FIFO_RG* register without address autoincrement feature, and the corresponding data transfer count
- DSP application enables DMA interrupt at the end of data array transfer
- DSP application sets *AMW_EN* bit of *DSP_AMWREN_RG* IOX register to the '1' state in order to activate host PCI-bus mastering data transfer
- DSP application waits for DMA interrupt occurs and clears *AMW_EN* bit of *DSP_AMWREN_RG* IOX register after DMA transfer has been completed.

Refer to original TI documentation for TMS320C6x DSP for details how to program the DSP on-chip DMA controllers.

Selection of TMS320C6415/C6416 external DSP on-chip interface for TORNADO-P6415/P6416

TORNADO-P6415/P6416 DSP systems allow to select particular external TMS320C6415/C6416 DSP on-chip interface (McBSP-1 or UTOPIA) for communication with external devices and peripherals via *TORNADO-P6415/P6416* on-board connectors and DCM sites.

CAUTION

TORNADO-P6414 DSP systems with TMS320C6414 DSP do not provide DSP on-chip UTOPIA interface and feature TMS320C6414 DSP on-chip McBSP1 serial port always enabled.

The reason for this selection is that McBSP-1 and UTOPIA external TMS320C6415/C6416 DSP on-chip interfaces share common IC package pins due to the pins lack.

Selection between McBSP-1 and UTOPIA external TMS320C6415/C6416 DSP on-chip interfaces is performed via *TORNADO-P6415/P6416* on-board SW4-3 configuration switch (fig. 2-1c and fig.A-1c) while DSP is in the reset state in accordance with table 2-14.

CAUTION

Altering the of SW4-3 switch state after DSP has been released from the reset state has no effect.

Table 2-14. Selection of TMS320C6415/C6416 external interface for *TORNADO-P6415/P6416* DSP systems.

SW4-3 switch	Description
ON	TMS320C6415/C6416 DSP on-chip McBSP-1 serial port interface is selected for communication with external devices/peripherals via *TORNADO-P6415/P6416* on-board SIOX-A rev.B (JP4), SIOX-A rev.C (JP2) and SIOX-B rev.C (JP3) DCM sites.
OFF	TMS320C6415/C6416 DSP on-chip 50MHz 8-bit UTOPIA level 2 slave ATM interface is selected for communication with external devices/peripherals via *TORNADO-P6415/P6416* on-board UTOPIA I/O connectors (JP14 and JP15).

Note: 1. Highlighted configuration corresponds to default factory setting.

DSP application for *TORNADO-P6415/P6416* DSP systems can define which particular external TMS320C6415/C6415 DSP on-chip interface has been selected by reading *UTOPIA_EN* read-only bit of *DSP_SYS_STAT_RG* IOX register (refer to the corresponding subsection above and to table 2-9). *UTOPIA_EN* read-only bit of *DSP_SYS_STAT_RG* IOX register is latched on release of DSP reset signal and does not change until new DSP reset condition is applied.

UTOPIA interface of TORNADO-P6415/P6416 DSP systems

TORNADO-P6415/P6416 DSP systems provide 8-bit UTOPIA level 2 slave interface for communication with external ATM master devices at speeds up to 50MHz per direction and user defined cell format up to 64 bytes.

UTOPIA interface is the part of TMS320C6415/C6416 DSP on-chip peripherals and can be selected alternatively to DSP on-chip McBSP1 serial port via on-board SW4-3 switch.

CAUTION

This manual does not contain description and programming details for TMS320C6415/C6416 DSP on-chip 8-bit UTOPIA level 2 slave ATM interface.

For more information refer to original TI datasheets and user's guide for TMS320C6x DSP, which are supplied in either paper or electronic form together with this manual.

Before using TMS320C6415/C6416 DSP on-chip UTOPIA interface of *TORNADO-P6415/P6416* DSP systems, it must be enabled via on-board SW4-1 configuration switch in accordance with table 2-14 while DSP

is in the reset state. This selection is required because McBSP-1 DSP on-chip serial port and UTOPIA DSP on-chip interface share common DSP IC package pins due to the pins lack (refer to the corresponding subsection above for more details). Note, that Altering the of SW4-3 switch state after DSP has been released from the reset state has no effect.

External UTOPIA ATM master device shall connect to *TORNADO-P6415/P6416* DSP systems via on-board JP15 (UTOPIA receiver) and JP14 (UTOPIA transmitter) connectors.

Pinout for *TORNADO-P6415/P6416* on-board UTOPIA I/O connectors are presented at figures 2-3a and 2-3b, and signal description is provided in table 2-15. All signal names for UTOPIA receiver and transmitter connector signals correspond to those from TI TMS320C6415/C6416 DSP datasheet.

CAUTION

All *TORNADO* DSP systems and controllers with TMS320C6415/C6416 DSP, which provide on-board support for TMS320C6415/C6416 DSP on-chip UTOPIA interface (i.e. *TORNADO-P6415/P6416/E6415/E6416*/etc), feature compatible on-board UTOPIA receiver and UTOPIA transceiver I/O connectors and interface signal specifications.

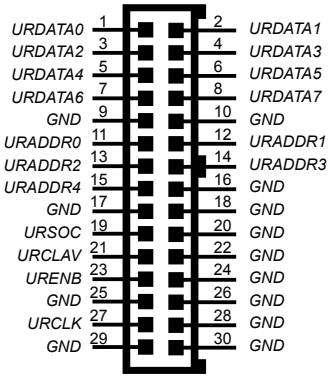


Fig.2-3a. Pinout for UTOPIA receiver connector (JP15) of *TORNADO-P6415/P6416* (top view).

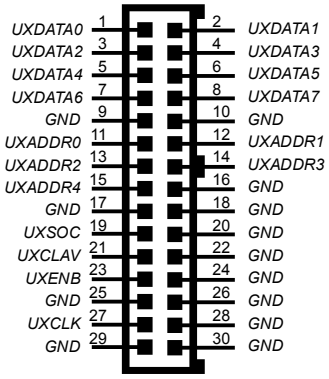


Fig.2-3b. Pinout for UTOPIA transmitter connector (JP14) of *TORNADO-P6415/P6416* (top view).

Table 2-15a. UTOPIA receiver connector signals for *TORNADO-P6415/P6416*.

Signal name	signal type	Description
URDATA[0..7]	I	Active high UTOPIA receiver 8-bit input data.
URADDR[0..4]	I	Active high UTOPIA receiver 5-bit input address.
URSOC	I	Active high UTOPIA receiver start of cell input.
URCLAV	O	Active high UTOPIA receiver cell available output from UTOPIA slave.
URENB	I	Active high UTOPIA receiver enable input.
URCLK	I	Active high UTOPIA receiver clock input.
GND	-	Ground.

Note: 1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
2. All logical signal levels and load currents correspond to that for 3v/5v TTL signals with *Iout*=16mA.

Table 2-15b. UTOPIA transmitter connector signals for *TORNADO-P6415/P6416*.

Signal name	signal type	Description
UXDATA[0..7]	O	Active high UTOPIA transmitter 8-bit input data.
UXADDR[0..4]	I	Active high UTOPIA transmitter 5-bit input address.
UXSOC	O	Active high UTOPIA transmitter start of cell output.
UXCLAV	O	Active high UTOPIA transmitter cell available output from UTOPIA slave.
UXENB	I	Active high UTOPIA transmitter enable input.
UXCLK	I	Active high UTOPIA transmitter clock input.
GND	-	Ground.

Note: 1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
2. All logical signal levels and load currents correspond to that for 3v/5v TTL signals with *Iout*=16mA.

CAUTION

All active high/low UTOPIA receiver and transmitter input signals are on-board terminated via pull-down/up 110 Ohm resistors correspondingly, which provides impedance match with 2mm flat cable for connection to external UTOPIA ATM master controller.

TORNADO-P6415/P6416 on-board UTOPIA receiver (JP15) and UTOPIA transmitter (JP14) connectors are Samtec STMM-115-02-G-D 30-pin 2mm male headers. The mating parts are Samtec TCSD-15-01-N female plugs for 2mm 30-wire flat cable, which are included as standard option with *TORNADO-P6415/P6416* DSP systems. Extra UTOPIA receiver/transmitter connector plugs are available either from Samtec Inc (www.samtec.com) or from MicroLAB Systems upon request.

TMS320C6x DSP on-chip timers

TORNADO-P62xx/P67 on-board TMS320C620x/C6701 DSP provides two DSP on-chip timers (TM0 and TM1), whereas *TORNADO-P64xx* on-board TMS320C64xx DSP provides three DSP on-chip timers (TM0, TM1 and TM2). For more details about TMS320C6x DSP on-chip timers refer to original TI documentation for TMS320C6x DSP.

TMS320C6x DSP on-chip timers control pins comprise of the timer input-only pins (TINP0, TINP1, and TINP2) and timer output-only pins (TOUT0, TOUT1, and TOUT2). Timer I/O pins can be used as either general purpose I/O pins or as timer I/O clock pins and are externally available via *TORNADO-P6x* on-board SIOX-A/B and PIOX/PIOX-16 DCM sites and on-board edge connector (DSP on-chip TM2 I/O pins for *TORNADO-P64xx* only). Figures 2-4a, 2-4b and 2-4c provides details about on-board connection of DSP on-chip timers for all *TORNADO-P6x* DSP systems.

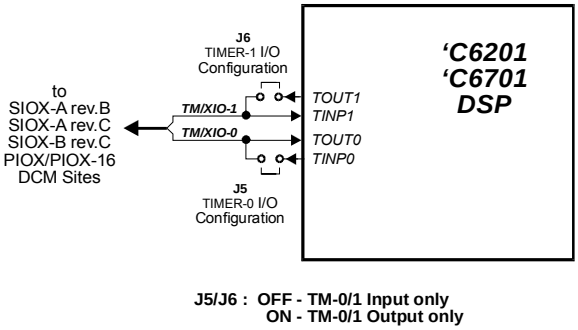


Fig. 2-4a. Connection diagram for DSP on-chip timers for *TORNADO-P62/P67* DSP systems.

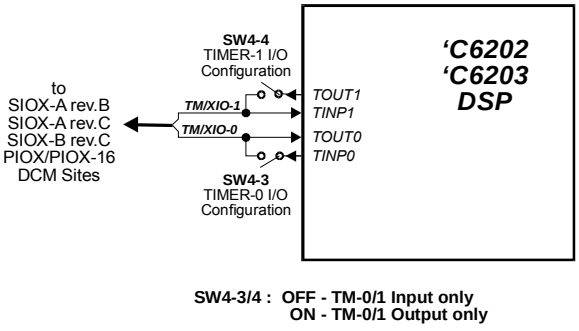


Fig. 2-4b. Connection diagram for DSP on-chip timers for *TORNADO-P6202/P6203* DSP systems.

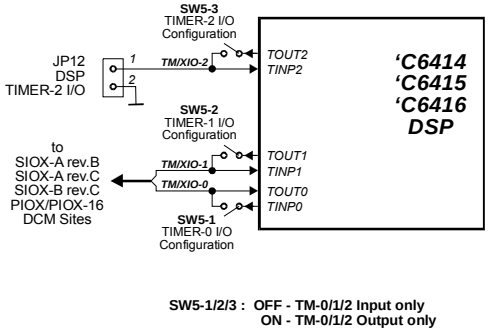


Fig. 2-4c. Connection diagram for DSP on-chip timers for *TORNADO-P64xx* DSP systems.

Selection between DSP on-chip timer input-only and timer output-only modes is performed via on-board jumpers J5 and J6 for ***TORNADO-P62/P67*** DSP systems, via on-board switches SW4-3 and SW4-4 for ***TORNADO-P6202/P6203*** DSP systems, and via on-board switches SW5-1, SW5-2 and SW5-3 for ***TORNADO-P64xx*** DSP systems. When either the corresponding jumper is not installed, or the corresponding

switch is in the 'OFF' state, then on-board *TM/XIO-n* signal is connected to the corresponding *TINPn* input pin of DSP on-chip timer #n (n=0..2), which corresponds to timer input-only or general purpose input-only mode. Vice-versa, in case either jumper is installed, or switch is in the 'ON' state, then on-board *TM/XIO-n* signal is connected to the corresponding both *TINPn* input and *TOUTn* output pins of DSP on-chip timer #n (n=0..2) , which corresponds to timer output-only or general purpose output-only mode with output read-back.

CAUTION

I/O configuration of TMS320C6x DSP on-chip timer I/O pins, which is set by DSP application via the corresponding DSP on-chip timer control register, must match configuration of the corresponding on-board J5/J6 jumpers (*TORNADO-P62/P67*), SW4-3/4 switches (*TORNADO-P6202/P6203*), and SW5-1/2/3 switches (*TORNADO-P64xx*), and it is not possible to dynamically reconfigure these pins at run-time via DSP software from timer/input-only to timer/output-only and vise-versa.

All *TORNADO-P6x* on-board external *TM/XIO-n* timer I/O signals are CMOS/TTL 3v/5v compatible I/O signals and provide I_L=1.6mA.

TM/XIO-0 and *TM/XIO-1* on-board timer/IO signals of all *TORNADO-P6x* DSP systems, which correspond to TMS320C6x DSP on-chip timer-0 (TM0) and timer-1 (TM1) I/O signals, are routed directly to on-board PIOX-16 and SIOX-A/B rev.B/C DCM site headers. Refer to the corresponding sections below in this chapter for more details.

TM/XIO-2 on-board timer/IO signal of *TORNADO-P64xx* DSP systems, which correspond to TMS320C64xx DSP on-chip timer-2 (TM0) I/O signals, is routed directly to on-board JP12 edge connector as shown at figure 2-4c and 2-5. *TORNADO-P64xx* on-board JP12 TM2 I/O connector is the industry standard 0.05" 2-pin male header from Molex (www.molex.com). The mating plugs are available from upon request from MicroLAB Systems.

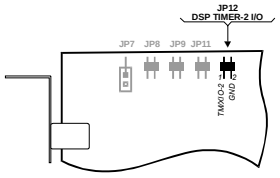


Fig. 2-5. Pinout of DSP on-chip timer-2 I/O connector for *TORNADO-P64xx* DSP systems (top view).

Maximum output clock frequency for TMS320C6x DSP on-chip timers is ¼-th of DSP clock frequency, which corresponds to 50 MHz for *TORNADO-P62* DSP systems, 41 MHz for *TORNADO-P67* DSP systems, 62.5 MHz for *TORNADO-P6202* DSP systems, 75 MHz for *TORNADO-P6203* DSP systems, and 150 MHz for all *TORNADO-P64xx* DSP systems.

DSP general purpose I/O (TORNADO-P64xx only)

TORNADO-P64xx DSP systems provide on-board 10-bit DSP general purpose I/O signals (*DSP_GPIO-0/3/8..15*), which are wired to on-board JP13 connector (refer to fig.2-2c and fig.A-1). General purpose I/O is

useful for interfacing to external sensors, switches, etc and for generation of local control signals in a variety of applications.

DSP_GPIO-0/3/8..15 signals are actually the corresponding general purpose I/O pins of *TORNADO-P64xx* on-board TMS320C64xx DSP, which are controlled via TMS320C64xx DSP on-chip GPEN, GPDIR, GPVAL, GPDL, GPDH, GPHM, GPLM, GPGC, and GPPOL registers. *DSP_GPIO-0/3/8..15* DSP general purpose I/O signals can be used for general purpose I/O, generation of DSP interrupt, and EDMA events.

CAUTION

For details about TMS320C64xx DSP on-chip general purpose I/O pins refer to original TI TMS320C6x DSP documentation, which is supplied in either electronic or paper form together with *TORNADO-P6x* DSP systems.

CAUTION

TORNADO-P64xx on-board TMS320C64xx DSP provide only *DSP_GPIO-0*, *DSP_GPIO-3*, and *DSP_GPIO-8..15* DSP on-chip general purpose I/O signals available for external I/O via on-board JP13 connector.

Other TMS320C64xx DSP on-chip general purpose I/O are reserved and shall not be configured as general purpose I/O pins via TMS320C64xx DSP on-chip GPEN register.

Pinout for *TORNADO-P64xx* on-board JP13 10-bit DSP general purpose I/O connector is presented at fig.2-6. Signal description corresponds to that provided in original TI TMS320C6x DSP datasheets and user's guides.

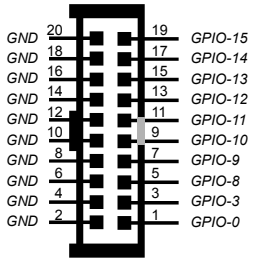


Fig. 2-6. Pinout for DSP general purpose I/O connector (JP13) of *TORNADO-P64xx* DSP systems (top view).

TORNADO-P64xx on-board *DSP_GPIO-0/3/8..15* DSP general purpose I/O signals are TTL 3v/5v compatible signals with I_L=3.2mA load current.

TORNADO-P64xx on-board JP13 DSP general purpose I/O connector is Samtec STMM-110-02-G-D 30-pin 2mm guarded male headers. The mating parts are Samtec TCSD-10-01-N female plugs for 2mm 20-wire flat cable, which are included as standard option with *TORNADO-P64xx* DSP systems. Extra DSP general purpose I/O plugs are available upon request from either Samtec Inc (www.samtec.com) or MicroLAB Systems.

External DSP reset input connector

TORNADO-P6x DSP systems provide on-board JP7 external DSP reset input connector (refer to figures 2-2 and A-1), which can be used in order to apply active low external DSP reset signal (*XRESET*) when on-board DSP is running in stand-alone operation mode.

CAUTION

External DSP reset input (*XRESET*) is ignored in case *TORNADO-P6x* on-board DSP is running in host PC operation mode.

Pinout for *TORNADO-P6x* on-board JP7 external DSP reset input connector is presented at figure 2-7. Note, that *XRESET* active low external DSP reset input is on-board pulled-up and is 3v/5v TTL compatible digital input.

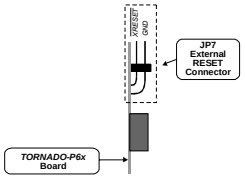


Fig. 2-7. Pinout of external DSP reset input connector (JP7) (side view).

TORNADO-P6x on-board JP7 external DSP reset connector is the industry standard 2-pin 0.1" pitch dual-row right-angle male header. Compatible 2-pin female plug is available from a variety of vendors including AMP, Molex, etc..

External power connector

In case *TORNADO-P6x* DSP system is used as stand-alone DSP controller and is not installed into host PCI-bus slot, then on-board external power connector JP10 (see fig.2-2 and fig.A-1) must be used to apply external power to *TORNADO-P6x* board.

External power connector (JP10) for *TORNADO-P6x* DSP system (refer to fig.2-2 and fig.A-1) comprises of +5v and ±12v power inputs. Figure 2-8 provides pinout for *TORNADO-P6x* on-board JP10 external power connector.

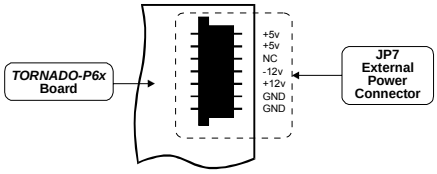


Fig. 2-8. Pinout of external power connector (JP10) (top view).

CAUTION

Only +5v external power supply input is required for operation of *TORNADO-P6x* on-board hardware.

External ±12v external power supply inputs and on-board –5v power are directly wired to on-board PIOX/PIOX-16 and SIOX-A/B rev.B/C DCM sites and are not used by *TORNADO-P6x* on-board hardware. If neither of PIOX/PIOX-16 and SIOX-A/B rev.B/C DCM is installed or does not consume –5v and ±12v power, then ±12v external power supply inputs can be left unconnected.

On-board –5v power for PIOX/PIOX-16 and SIOX-1/B rev.B/C DCM sites is derived from either PCI-bus –12v power supply source (in case *TORNADO-P6x* board is installed into host PCI-bus slot) or external –12v power supply source, which is applied via on-board JP10 external power input connector (in case *TORNADO-P6x* board is not installed into host PCI-bus slot).

External power connector of *TORNADO-P6x* DSP systems is the industry standard 7-pin 0.1" pitch single-row right-angle male power header, which is available from a variety of vendors including AMP, Molex, etc. One piece of the mating power plug is included as the standard option with *TORNADO-P6x* board. Extra power plugs are available from ether from MicroLAB Systems upon request, or from AMP, Molex and other manufacturers.

2.3 Host PCI-bus Interface

Host PCI-bus interface of *TORNADO-P6x* DSP systems has been designed for bi-directional data transfer between host PCI-bus and DSP environments via bi-directional FIFO, bi-directional mailboxes, high density DPRAM, DSP on-chip HPI port and mutual interrupts, for *TORNADO-P6x* DSP and system control, and for emulation control of on-board TMS320C6x DSP via on-board emulation controller chip (ECC) and DSP-on-chip JTAG port.

Host PCI-bus interface architecture

TORNADO-P6x host PCI-bus interface (fig.2-1) has been designed using industry standard primary AMCC S5933 PCI controller (*PCIC*) for direct connection to host PCI-bus, and secondary FPGA for control of add-on peripherals (HIF registers, ECC, SB access buffers, etc), which are connected to the local output bus of AMCC S5933 PCIC (PCIC AOB).

CAUTION

For more details about *TORNADO-P6x* on-board AMCC S5933 PCIC refer to Appendix B of this manual and to original AMCC S5933 PCIC User's Guide, which is included in either paper or electronic form along with this manual.

TORNADO-P6x host PCI-bus interface occupies four independent PCI-bus I/O areas, which are allocated into memory and I/O address spaces of host PCI-bus (refer to the corresponding subsection below for more details). Each area of host PCI-bus interface corresponds to particular on-board peripheral(s) directly controlled via host PCI-bus.

TORNADO-P6x host PCI-bus interface supports direct access to AMCC S5933 PCIC on-chip AOB operation registers from on-board TMS320C6x DSP for communication between on-board DSP and host PCI-bus via bidirectional FIFO and a set of bidirectional mailboxes, which are on the other side visible by host PC application via AMCC S5933 PCIC on-chip PCI operation registers. For more details refer to section "TMS320C6x DSP Environment" earlier in this chapter.

TORNADO-P6x host PCI-bus interface supports DSP controlled PCI-bus mastering transfers to and from DSP environment. This provides 'transparent visibility' of full PCI-bus memory and I/O address spaces for *TORNADO-P6x* on-board DSP, 'virtually expands' *TORNADO-P6x* on-board memory resources, and allows real-time communication between *TORNADO-P6x* on-board DSP and installed PCI-bus devices (including other *TORNADO* PCI-bus plug-in DSP systems).

Host PCI-bus interface areas

TORNADO-P33 host PCI-bus interface occupies four independent I/O areas, which are directly mapped host PCI-bus memory and I/O address spaces (table 2-16). Each area corresponds to particular on-board peripheral(s) directly controlled via host PCI-bus.

Table 2-16. Host PCI-bus interface areas.

Host PCI-bus interface area	**PCI base address configuration register**	**Area size**	**Area allocation**
AMCC S5933 PCIC on-chip PCI operation registers area	BADDR0	64 bytes	32-bit I/O
ECC JTAG emulator interface area	BADDR1	128 bytes	16-bit I/O
Reserved	BADDR2	-	-
DPRAM/DPSEM area with paged memory (SMP) access (TORNADO-P62xx/P67 only)	BADDR3	32 kbytes	32-bit memory below 1MB (UMB memory area) [1)] or 32-bit memory in 32-bit memory address space of PCI-bus [1)]
DPRAM area without paged memory access (TORNADO-P64xx only)	BADDR3	512 kbytes (128Kx32 DPRAM) [2)] 1 Mbytes (256Kx32 DPRAM) [2)] or 32 kbytes [2)]	32-bit memory in 32-bit memory address space of PCI-bus [2)] 32-bit memory below 1MB (UMB memory area) [2)]
host interface (HIF) registers and DSP HPI port area	BADDR4	64 bytes	16-bit I/O (*TORNADO-P62/P67*) 32-bit I/O (*TORNADO-P6202/P6203/P64xx*)

Note: 1. Allocation of 32 kbytes memory page for access to on-board DPRAM with paged access in host PCI-bus memory space for *TORNADO-P62xx/P67* DSP systems is configured via host PC utilities (*TP_DP1M.EXE* and *TP_DP32.EXE*).
2. Size of on-board DPRAM memory page (either 32 kbytes or full DPRAM capacity) and its allocation in the PCI-bus memory space for *TORNADO-P64xx* DSP systems is configured via host PC utilities (*TP_DP1M.EXE* and *TP_DP32.EXE*).

Particular PCI-bus memory/IO base address for each area of *TORNADO-P6x* host PCI-bus interface, i.e. the contents of BADDR0..BADDR4 PCI-bus configuration registers, are assigned by host PCI BIOS during PC boot procedure in accordance with AMCC S5933 PCIC start-up configuration, which is loaded from on-board serial EEPROM/nvRAM.

CAUTION

Host PC application does not need to access BADDR0..BADDR4 PCI-bus configuration registers of AMCC S5933 PCIC in order to get memory/IO base for particular PCI-bus area, since these PCI-bus configuration registers are automatically handled by *TORNADO-P6x* DOS utilities and *TORNADO Software Development Kit* (*TSDK*) software for Windows.

TORNADO-P6x DSP systems use on-board 2Kx8 serial EEPROM (nvRAM) in order to store AMCC S5933 PCIC start-up configuration and user defined non-volatile data.

CAUTION

First 128 bytes of 2Kx8 serial EEPROM contain AMCC S5933 PCIC start-up configuration and shall not be modified by user DSP and/or host applications, which can write to EEPROM (nvRAM). Unauthorized modification of AMCC S5933 PCIC start-up configuration in on-board serial EEPROM/nvRAM will result in incorrect operation of *TORNADO-P6x* host PCI-bus interface.

User DSP and/or host application can use 0x80..0x7ff address locations of on-board serial EEPROM/nvRAM to store user defined data.

AMCC S5933 PCIC on-chip PCI operation registers area of *TORNADO-P6x* host PCI-bus interface comprises of a set of on-chip control/status registers, which are used for communication between host PC application and DSP application via bidirectional FIFO, bidirectional mailboxes, and DSP-to-host interrupt request. For more details refer to the corresponding subsection below.

DPRAM/DPSEM access area of *TORNADO-P6x* host PCI-bus interface is used for host-to-DPRAM and host-to-DPSEM accesses (*TORNADO-P62xx/P67* only) for communication host PC application and DSP application via dual-port RAM and dual-port semaphores (*TORNADO-P62xx/P67* only). *TORNADO-P62xx/P67* DSP systems use memory paging method to access on-board DPRAM for compatibility with old *TORNADO* DSP systems, whereas *TORNADO-P64xx* DSP systems provide direct mapping of full on-board DPRAM to PCI-bus 32-bit memory address space for performance reasons. For more details about DPRAM/DPSEM area of *TORNADO-P6x* host PCI-bus interface refer to the corresponding subsection below.

Host interface (HIF/HPI) registers area of *TORNADO-P6x* host PCI-bus interface is used for *TORNADO-P6x* on-board DSP control, for communication between host PC and DSP applications via mailboxes and mutual interrupts, for selection of DPRAM access page, and for access to DSP environment via DSP on-chip HPI port. For more details refer to the corresponding subsection below.

ECC JTAG emulator interface area of *TORNADO-P6x* host PCI-bus interface is used for control of on-board *ECC* emulation controller when debugging on-board TMS320C6x DSP application via DSP on-chip JTAG port using TI C6000 Code Composer Studio debugger.

CAUTION

This manual does not provide details for *ECC* JTAG emulator interface area of *TORNADO-P6x* host PCI-bus interface, since this information is not intended for user host PC application programming and is handled by *TORNADO-P6x* host DOS utilities, by *TORNADO Software Development Kit* (*TSDK*), and by *TORNADO-P6x ECC* emulator driver for TI C6000 Code Composer Studio debug tools.

AMCC S5933 PCIC on-chip PCI operation registers area

AMCC S5933 PCIC on-chip PCI operation registers area of *TORNADO-P6x* host PCI-bus interface is used for communication between host PCI-bus and on-board DSP via PCIC on-chip bidirectional FIFO and a set of bidirectional mailboxes, and to control PCI-bus interrupt request.

CAUTION

This subsection contains brief information about AMCC S5933 PCIC on-chip PCI operation registers.

For more details about *TORNADO-P6x* on-board AMCC S5933 PCIC refer to Appendix B of this manual and to original AMCC S5933 PCIC User's Guide, which is included in either paper or electronic form along with this manual.

AMCC S5933 PCIC on-chip PCI operation registers area of *TORNADO-P6x* host PCI-bus interface comprises of 16 32-bit control/status register and is mapped into host PCI-bus 32-bit I/O area.

CAUTION

Particular PCI-bus I/O base address for AMCC S5933 PCIC on-chip PCI operation registers are of *TORNADO-P6x* host PCI-bus memory interface is assigned by host PCI BIOS during PC boot procedure, and, if it is required, can be obtained by host PC application by reading AMCC S5933 PCIC on-chip BADDR-0 PCI-bus configuration register.

Host PC application does not normally need to read BADDR0..BADDR4 PCI-bus configuration registers of AMCC S5933 PCIC in order to get memory/IO base for particular PCI-bus area, since these PCI-bus configuration registers are automatically handled by *TORNADO-P6x* DOS utilities and *TORNADO Software Development Kit* (*TSDK*) utility software for Windows.

CAUTION

AMCC S5933 PCIC on-chip PCI operation registers area of *TORNADO-P6x* host PCI-bus interface can be accessed from host PCI-bus only without any wait states applied.

Table 2-17 provides a list of 32-bit control/status registers, which are available via AMCC S5933 PCIC on-chip PCI operation registers area of *TORNADO-P6x* host PCI-bus interface.

Table 2-17. AMCC S5933 PCIC on-chip PCI Operation Registers Area of host PCI-bus interface.

register name	register address	data bits	access mode	PC reset value	Description
HOST_PCIC_FIFO_RG	*BADDR0*+20H	32	r/w	-	PCIC read/write FIFO register (read: read-FIFO, write: write-FIFO).
HOST_PCIC_MBEF_RG	*BADDR0*+34H	32	r	0x00000000	PCIC PCI-bus mailbox empty/full status register
HOST_PCIC_INTCSR_RG	*BADDR0*+38H	32	r/w	0x00000000	PCIC PCI-bus interrupt control/status register
HOST_PCIC_MCSR_RG	*BADDR0*+3CH	32	r/w	0x000000E6	PCIC PCI-bus master control/status register
HOST_PCIC_MWAR_RG	*BADDR0*+24H	32	r	0x00000000	PCIC PCI-bus master write address register. This register is not available for write operation from host PCI-bus interface, since *TORNADO-P6x* on-board AMCC S5933 PCIC is configured for DSP controlled PCI-bus mastering transfers.
HOST_PCIC_MWTC_RG	*BADDR0*+28H	32	r	0x00000000	PCIC PCI-bus master write transfer counter register. This register is not available for write operation from host PCI-bus interface, since *TORNADO-P6x* on-board AMCC S5933 PCIC is configured for DSP controlled PCI-bus mastering transfers.
HOST_PCIC_MRAR_RG	*BADDR0*+2CH	32	r	0x00000000	PCIC PCI-bus master read address register. This register is not available for write operation from host PCI-bus interface, since *TORNADO-P6x* on-board AMCC S5933 PCIC is configured for DSP controlled PCI-bus mastering transfers.

HOST_PCIC_MRTC_RG	*BADDR0*+30H	32	r	0x00000000	PCIC PCI-bus master read transfer counter register. This register is not available for write operation from host PCI-bus interface, since *TORNADO-P6x* on-board AMCC S5933 PCIC is configured for DSP controlled PCI-bus mastering transfers.
HOST_PCIC_IMBX0_RG *HOST_PCIC_IMBX1_RG* *HOST_PCIC_IMBX2_RG* *HOST_PCIC_IMBX3_RG*	*BADDR0*+10H *BADDR0*+14H *BADDR0*+18H *BADDR0*+1CH	32	r	-	PCIC PCI-bus incoming mailbox registers #1..#4
HOST_PCIC_OMBX0_RG *HOST_PCIC_OMBX1_RG* *HOST_PCIC_OMBX2_RG* *HOST_PCIC_OMBX3_RG*	*BADDR0*+00H *BADDR0*+04H *BADDR0*+08H *BADDR0*+0CH	32	r/w	-	PCIC PCI-bus outgoing mailbox registers #1..#4

Notes: 1. '*BADDR0*' denotes I/O base address of AMCC S5933 PCIC PCI operation registers area of host PCI-bus interface in accordance with table 2-16.
2. Register access modes: *r* - read only, *w* - write only, *r/w* - read/write.

CAUTION

For details about AMCC S5933 PCIC on-chip PCI operation registers format refer to Appendix B of this manual and to AMCC S5933 PCIC User's Guide, which is supplied in either paper or electronic form along with this manual.

CAUTION

Access from host PCI-bus to all AMCC S5933 PCIC on-chip 32-bit PCI operation registers except for ***HOST_PCIC_FIFO_RG*** register can be performed using 8-/16-/32-bit data access cycles.

Access from host PCI-bus to AMCC S5933 PCIC on-chip 32-bit ***HOST_PCIC_FIFO_RG*** operation registers must be performed using 32-bit data access cycles only.

32-bit read/write ***HOST_PCIC_FIFO_RG*** PCIC on-chip PCI operation register is used for 'stream'-type bidirectional communication between host PCI-bus and ***TORNADO-P6x*** on-board DSP via 8-level bidirectional FIFO (first-in/first-out). When host PC application writes to ***HOST_PCIC_FIFO_RG*** AMCC S5933 PCIC on-chip PCI operation register of host PCI-bus interface, then written data is put into host-to-DSP 8-level FIFO queue and DSP can read transferred data via ***DSP_PCIC_FIFO_RG*** PCIC on-chip AOB operation register (refer to Appendix B of this manual and to section "TMS320C6x DSP Environment" earlier in this chapter) using first-in/first-out algorithm. Once data has been read from FIFO, then it is lost and internal

FIFO data is shifted. Vice-versa, when DSP writes to ***DSP_PCIC_FIFO_RG*** PCIC AOB operation register, then written data is put into DSP-to-host 8-level FIFO queue and host PC application can read transferred data from ***HOST_PCIC_FIFO_RG*** AMCC S5933 PCIC on-chip PCI operation register of host PCI-bus interface using first-in/first-out algorithm.

CAUTION

Before reading/writing from/to ***HOST_PCIC_FIFO_RG*** AMCC S5933 PCIC on-chip PCI operation register, host PC application must check FIFO status via ***DSP_PCIC_MCSR_RG*** AMCC S5933 PCIC on-chip PCI operation register in order to ensure that read FIFO contains valid data and that write FIFO has at least one empty location.

PCIC FIFO status flags can be cleared either by DSP via ***DSP_PCIC_AGCSTS_RG*** AMCC S5933 PCIC on-chip AOB operation register, or by host PC application via ***HOST_PCIC_MCSR_RG*** AMCC S5933 PCIC on-chip PCI operation register of host PCIC area of host PCI-bus interface.

HOST_PCIC_FIFO_RG AMCC S5933 PCIC on-chip PCI operation register is also used DSP-to-host and host-to-DSP data transfers during DSP controlled PCI-bus mastering mode (refer to section "TMS320C6x DSP Environment" earlier in this chapter for more details).

Read/write ***HOST_PCIC_OMBX0_RG..HOST_PCIC_OMBX3_RG*** AMCC S5933 PCIC on-chip PCI operation registers are used as 32-bit outgoing mailboxes for data transfer from host PC application to ***TORNADO-P6x*** on-board DSP. ***HOST_PCIC_OMBX0_RG..HOST_PCIC_OMBX3_RG*** AMCC S5933 PCIC on-chip PCI operation registers are name alias for OMB1..OMB4 PCIC PCI operation registers correspondingly in accordance with Appendix B of this manual and AMCC S5933 PCIC User's Guide. When host PC application writes to any of ***HOST_PCIC_OMBX0_RG.. HOST_PCIC_OMBX3_RG*** registers of host PCIC area of host PCI-bus interface, then DSP can read written data via corresponding ***DSP_PCIC_IMBX0_RG..DSP_PCIC_IMBX3_RG*** PCIC AOB operation registers (refer to Appendix B of this manual and to section "TMS320C6x DSP Environment" earlier in this chapter). Host PC application can read back ***HOST_PCIC_OMBXn_RG*** AMCC S5933 PCIC on-chip PCI outgoing mailbox registers without loosing register data, and DSP can read ***DSP_PCIC_IMBXn_RG*** AOB incoming mailbox registers as many times as required by DSP application without loosing incoming mailbox register data, however AMCC S5933 PCIC on-chip AOB incoming mailbox data ready flags, which are available via ***DSP_PCIC_AMBEF_RG*** PCIC AOB operation register and ***HOST_PCIC_MBEF_RG*** host PCI-bus operation register, will be reset after first read from ***DSP_PCIC_IMBXn_RG*** PCIC AOB register.

Read-only ***HOST_PCIC_IMBX0_RG..HOST_PCIC_IMBX3_RG*** AMCC S5933 PCIC on-chip PCI operation registers are used as 32-bit incoming mailboxes for data transfer from ***TORNADO-P6x*** on-board DSP to host PC application. ***HOST_PCIC_IMBX0_RG..HOST_PCIC_IMBX3_RG*** AMCC S5933 PCIC on-chip PCI operation registers are name alias for IMB1..IMB4 AMCC S5933 PCIC on-chip PCI operation registers correspondingly in accordance with Appendix B of this manual and AMCC S5933 PCIC User's Guide. When DSP writes to any of ***DSP_PCIC_OMBX0_RG..DSP_PCIC_OMBX3_RG*** AMCC S5933 PCIC on-chip AOB operation register (refer to Appendix B of this manual and to section "TMS320C6x DSP Environment" earlier in this chapter), then host PC application can read written data via corresponding read-only ***HOST_PCIC_IMBX0_RG..HOST_PCIC_IMBX3_RG*** registers of AMCC S5933 PCIC PCI operation registers area of host PCI-bus interface. Host PC application can read ***HOST_PCIC_IMBXn_RG*** incoming

mailbox registers as many times as required by host application without loosing incoming mailbox register data, however host PCI-bus incoming mailbox data ready flags, which are available via *HOST_PCIC_MBEF_RG* AMCC S5933 PCIC on-chip PCI operation register, will be reset after first read from *HOST_PCIC_IMBXn_RG* register.

CAUTION

TORNADO-P6x on-board AMCC S5933 PCIC is configured with byte #3 of *DSP_PCIC_OMBX3_RG* AMCC S5933 PCIC on-chip AOB outgoing mailbox register and corresponding *HOST_PCIC_IMBX3_RG* AMCC S5933 PCIC on-chip PCI incoming mailbox register being used for generation of host PCI-bus interrupt.

This results in masking out most significant byte data when DSP writes to *DSP_PCIC_OMBX3_RG* AMCC S5933 PCIC on-chip AOB operation register, and in undefined returned data for most significant byte data when host reads from *HOST_PCIC_IMBX3_RG* AMCC S5933 PCIC on-chip PCI incoming mailbox register.

Refer to Appendix B of this manual, original documentation for AMCC S5933 PCIC, the corresponding subsection below and to section "Host PCI-bus Interface" later in this chapter for more details.

HOST_PCIC_MWAR_RG, HOST_PCIC_MRAR_RG, HOST_PCIC_MWTC_RG and *HOST_PCIC_MRTC_RG* AMCC S5933 PCIC on-chip PCI operation registers can be used in read-only mode for status monitoring of DSP controlled PCI-bus mastering procurement, since AMCC S5933 PCIC of *TORNADO-P6x* host PCI-bus controller is configured for DSP controlled PCI-bus mastering. The mirrors of these AMCC S5933 PCIC on-chip PCI operation registers on the DSP side are *DSP_PCIC_MWAR_RG, DSP_PCIC_MRAR_RG, DSP_PCIC_MWTC_RG* and *DSP_PCIC_MRTC_RG* PCIC AOB operation registers, which can be read/written by *TORNADO-P6x* on-board DSP in order to configure DSP controlled PCI-bus mastering (refer to section "TMS320C6x DSP Environment" earlier in this chapter for more details).

HOST_PCIC_INTCSR_RG AMCC S5933 PCIC on-chip PCI operation register must be used to configure host PCI-bus interrupt request source and clear interrupt request flag (for more details refer to Appendix B of this manual and to original AMCC S5933 PCIC User's Guide).

HOST_PCIC_MCSR_RG AMCC S5933 PCIC on-chip PCI operation register must be used to monitor PCIC FIFO status, clear FIFO flags, and to control access to *TORNADO-P6x* on-board PCIC configuration NvRAM (EEPROM) (for more details refer to Appendix B of this manual and to original AMCC S5933 PCIC User's Guide).

DPRAM/DPSEM area of TORNADO-P62xx/P67 DSP systems

DPRAM/DPSEM area of *TORNADO-P62xx/P67* host PCI-bus interface is designed for communication between the host PCI-bus masters and on-board DSP environment via DPRAM memory and DPSEM hardware semaphores.

CAUTION

Refer to section “TMS320C6x DSP Environment” earlier in this chapter and to table 2-4 for more details about DPSEM hardware semaphores.

TORNADO-P62xx/P67 DSP systems use memory paging method in order to access on-board 32Kx32 or 64Kx32 DPRAM memory and eight DPSEM hardware semaphores from host PCI-bus interface via 32 kbyte DPRAM shared memory page (SMP). DPRAM SMP appears as DPRAM area of *TORNADO-P62xx/P67* host PCI-bus interface and is mapped to host PCI-bus memory space. Particular selection of 32 kbyte DPRAM memory page within DPRAM memory bank, which is accessed via DPRAM area of *TORNADO-P62xx/P67* host PCI-bus interface, is defined via DPRAM SMP registers (*HIF_SMP0_RG* and *HIF_SMP1_RG* HIF registers of host PCI-bus interface).

Memory paging method provides upward compatibility with host interface of all *TORNADO* PC plug-in DSP systems (including *TORNADO* DSP systems for host ISA-bus) with different type of memory, which is used in host PC interface (either shared memory or DPRAM) for communication between host PC interface and on-board DSP environment.

CAUTION

Allocation of 32 kbyte DPRAM SMP area of *TORNADO-P62xx/P67* host PCI-bus interface either into PC UMB memory area (below 1 Mbyte) or into PCI-bus 32-bit memory address area (above 1 Mbyte) can be configured via supplied PC DOS utilities (*TP_DP1M.EXE* and *TP_DP32.EXE*).

Memory paging method, which used to access on-board DPRAM/DPSEM resources from host PCI-bus interface for *TORNADO-P62xx/P67* DSP systems is supported by both *TORNADO-P6x* 16-bit DOS utilities and *TORNADO Software Development Kit* (*TSDK*) software for Windows.

CAUTION

In case 32 kbyte DPRAM SMP area of *TORNADO-P62xx/P67* host PCI-bus interface is allocated into PC UMB memory area (below 1 Mbyte), then this DPRAM area configuration is supported by both *TORNADO-P6x* 16-bit DOS utilities and *TORNADO Software Development Kit* (*TSDK*) software for Windows.

In case 32 kbyte DPRAM SMP area of *TORNADO-P62xx/P67* host PCI-bus interface is allocated into PCI-bus 32-bit memory address space (above 1 Mbyte), then this DPRAM area configuration is supported by *TORNADO Software Development Kit* (*TSDK*) software for Windows only.

CAUTION

The PCI-bus memory base address for DPRAM/DPSEM area is assigned by host PCI BIOS during PC boot procedure, and, if it is required, can be obtained by host PC application by reading AMCC S5933 PCIC on-chip BADDR-3 PCI-bus configuration register.

Host PC application does not normally need to read BADDR0..BADDR4 PCI-bus configuration registers of AMCC S5933 PCIC in order to get memory/IO base for particular PCI-bus area, since these PCI-bus configuration registers are automatically handled by *TORNADO-P6x* DOS utilities and *TORNADO Software Development Kit* (*TSDK*) software for Windows.

Once host PCI-bus executes memory access cycle within PCI-bus address range of 8Kx32 DPRAM/DPSEM memory area of *TORNADO-P62xx/P67* host PCI-bus interface, then the particular selected area (DPRAM or DPSEM) and particular DPRAM memory page are defined by *HIF_SMP0_RG* and *HIF_SMP1_RG* HIF registers from HIF/HPI area of *TORNADO-P62xx/P67* host PCI-bus interface (refer to the corresponding subsection below).

Below is the data format for the *HIF_SMP0_RG* and *HIF_SMP1_RG* HIF registers from HIF/HPI area of *TORNADO-P62xx/P67* host PCI-bus interface:

***HIF_SMP0_RG register* (r/w)**

bit-7	bit-6	bit-5	bit-4	Bit-3	bit-2	bit-1	bit-0
DPSEM_AREA (r/w, 0+)	*DP_MODE (r/w, 0+)*	*0*	*0*	*PG3 (r/w, 0+)*	*PG2 (r/w, 0+)*	*PG1 (r/w, 0+)*	*PG0 (r/w, 0+)*

HIF_SMP1_RG register (r/w)

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
DPSEM_AREA (r/w, 0+)	*0*	*0*	*0*	*PG3 (r/w, 0+)*	*PG2 (r/w, 0+)*	*PG1 (r/w, 0+)*	*PG0 (r/w, 0+)*

Table 2-18 provides details about *HIF_SMP0_RG* and *HIF_SMP1_RG* HIF registers bits for *TORNADO-P62xx/P67* DSP systems.

Table 2-18. Register bits of *HIF_SMP0_RG* and *HIF_SMP1_RG* registers for *TORNADO-P62xx/P67* DSP systems.

register bits	access mode	value on PC reset	Description
DPSEM_AREA	r/w	0	Selects area (either DPRAM or DPSEM) for PCI-bus accesses to DPRAM/DPSEM memory area of host PCI-bus interface of *TORNADO-P62xx/P67* DSP systems (table 2-19). *DPSEM_AREA* =0 selects DPRAM area for PCI-bus accesses to DPRAM/DPSEM memory area of host PCI-bus interface of *TORNADO-P62xx/P67* DSP systems. *DPSEM_AREA* =1 selects DPSEM area for PCI-bus accesses to DPRAM/DPSEM memory area of host PCI-bus interface of *TORNADO-P62xx/P67* DSP systems.
DP_MODE	r/w	0	Selects access mode (either dual-page or single-page) for PCI-bus accesses to the DPRAM/DPSEM memory area of host PCI-bus interface of *TORNADO-P62xx/P67* DSP systems (table 2-19). *DP_MODE* =0 selects single-page DPRAM/DPSEM access mode. *DP_MODE* =1 selects dual-page DPRAM/DPSEM access mode.
{*PG3..PG0*}	r/w	{0,0,0,0}	Selects DPRAM memory page for PCI-bus accesses to DPRAM/DPSEM memory area of host PCI-bus interface of *TORNADO-P62xx/P67* DSP systems.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on PC reset condition.

DPRAM/DPSEM area of host PCI-bus interface of *TORNADO-P62xx/P67* DSP systems can be configured to operate either in *single-page* or *dual-page* mode, which is defined by the *DP_MODE* bit of *HIF_SMP0_RG* HIF register.

CAUTION

Single-page mode is selected in case the *DP_MODE* bit of *HIF_SMP0_RG* HIF register of *TORNADO-P62xx/P67* DSP systems is set to the '0' state, which is also the default setting on PC power-on.

Single-page mode assumes that particular selected area (DPRAM or DPSEM) and particular accessed DPRAM memory page are defined by the contents of *HIF_SMP0_RG* register only (refer to table 2-15). *HIF_SMP1_RG* register is not used in *single-page mode*.

Single-page mode can be used in case there is only one external PCI-bus master, which communicates with *TORNADO-P62xx/P67* on-board TMS320C620xx/C6701 DSP via full 8Kx32 DPRAM/DPSEM area of *TORNADO-P62xx/P67* host PCI-bus interface.

CAUTION

Dual-page mode is selected in case the ***DP_MODE*** bit of ***HIF_SMP0_RG*** HIF register of ***TORNADO-P62xx/P67*** DSP systems is set to the '1' state.

Dual-page mode denotes that in case host PCI-bus accesses the lower 4Kx32 sub-area of 8Kx32 DPRAM/DPSEM area, then particular selected area (DPRAM or DPSEM) and particular accessed DPRAM memory page are defined by the contents of ***HIF_SMP0_RG*** register (refer to table 2-19). Otherwise, in case host PCI-bus accesses the upper 4Kx32 sub-area of 8Kx32 DPRAM/DPSEM area, then particular selected area (DPRAM or DPSEM) and particular accessed DPRAM memory page are defined by the contents of ***HIF_SMP1_RG*** register (refer to table 2-19).

Dual-page mode is a recommended selection in case there are two and more external PCI-bus masters, which communicate with ***TORNADO-P62xx/P67*** on-board TMS320C620x/C6701 DSP via 4Kx32 sub-areas of DPRAM/DPSEM area of ***TORNADO-P62xx/P67*** host PCI-bus interface.

DPSEM_AREA bits of ***HIF_SMP0_RG*** and ***HIF_SMP1_RG*** registers define whether the DPRAM or DPSEM area is selected during PCI-bus access to DPRAM/DPSEM area of ***TORNADO-P62xx/P67*** host PCI-bus interface in accordance with table 2-19.

Table 2-19. DPRAM/DPSEM area selector via *HIF_SMP0_RG* and *HIF_SMP1_RG* registers of *TORNADO-P62xx/P67* DSP systems.

DP_MODE **bit of** ***HIF_SMP0_RG*** **register**	***DPSEM_AREA*** **bit of** ***HIF_SMP0_RG*** **register**	***DPSEM_AREA*** **bit of** ***HIF_SMP1_RG*** **register**	***A14 address bit of host PCI-bus***	**DPRAM/DPSEM Area**
Single-page DPRAM/DPSEM access mode via HIF_SMP0_RG register				
0	0	X	x	*DPRAM sub-area is selected via HIF_SMP0_RG register in single-page mode*: Bits *PG2..PG0* (for 64Kx32 DPRAM capacity) or bits *PG1..PG0* (for 32Kx32 DPRAM capacity) of *HIF_SMP0_RG* register define 8Kx32 DPRAM page, which is selected during PCI-bus access to the 8Kx32 DPRAM/DPSEM area of host PCI-bus interface of *TORNADO-P62xx/P67* DSP systems.
0	1	X	x	*DPSEM sub-area is selected via HIF_SMP0_RG register in single-page mode*: Bits *PG0..PG3* are ignored and DPSEM hardware semaphores are selected during PCI-bus access to 8Kx32 DPRAM/DPSEM area of host PCI-bus interface of *TORNADO-P62xx/P67* DSP systems. DPSEM appear as eight 32-bit words with D0 bit valid only.

Dual-page DPRAM/DPSEM access mode				
1	0	X	0	*DPRAM sub-area is selected via HIF_SMP0_RG register in dual-page mode*: Bits *PG3..PG0* (for 64Kx32 DPRAM capacity) or bits *PG2..PG0* (for 32Kx32 for DPRAM capacity) of *HIF_SMP0_RG* register define 4Kx32 DPRAM page, which is selected during PCI-bus access.
1	1	X	0	*DPSEM sub-area is selected via HIF_SMP0_RG register in dual-page mode*: Bits *PG0..PG3* of *HIF_SMP0_RG* register are ignored and DPSEM hardware semaphores are selected during PCI-bus access. DPSEM appear as eight 32-bit words with D0 bit valid only.
1	x	0	1	*DPRAM sub-area is selected via HIF_SMP1_RG register in dual-page mode*: Bits *PG3..PG0* (for 64Kx32 DPRAM capacity) or bits *PG2..PG0* (for 32Kx32 for DPRAM capacity) of *HIF_SMP1_RG* register define 4Kx32 DPRAM page, which is selected during PCI-bus access.
1	x	1	1	*DPSEM sub-area is selected via HIF_SMP1_RG register in dual-page mode*: Bits *PG0..PG3* of *HIF_SMP1_RG* register are ignored and DPSEM hardware semaphores are selected during PCI-bus access. DPSEM appear as eight 32-bit words with D0 bit valid only.

Note: 1. Highlighted configuration is set as default on host PC reset condition.

The following are several examples of how to set ***HIF_SMP0_RG*** and ***HIF_SMP1_RG*** registers and DPRAM/DPSEM page address when accessing DPRAM/DPSEM area of ***TORNADO-P62xx/P67*** host PCI-bus interface:

- Example 1: Host PC software needs to access location #0x100 (byte address) of DPRAM using single-page DPRAM/DPSEM access mode. The corresponding PC memory address will be (*BADDR3* + 0x100), and ***HIF_SMP0_RG*** register must be set to the 0x00 value.
- Example 2: Host PC software needs to access location #0x10040 (byte address) of DPRAM using single-page DPRAM/DPSEM access mode. The corresponding PC memory address will be (*BADDR3* + 0x40), and ***HIF_SMP0_RG*** register must be set to the 0x02 value.
- Example 3: Host PC software needs to access location #0x10040 (byte address) of DPRAM using dual-page DPRAM/DPSEM access mode via sub-page #0 (using ***HIF_SMP0_RG*** register). The corresponding PC memory address will be (*BADDR3* + 0x40), and ***HIF_SMP0_RG*** register must be set to the 0x44 value.
- Example 4: Host PC software needs to access location #0x17040 (byte address) of DPRAM using dual-page DPRAM/DPSEM access mode via sub-page #1 (using ***HIF_SMP1_RG*** register). The corresponding PC memory address will be (*BADDR3* + 0x3040), bit D6 of ***HIF_SMP0_RG*** register must be set to the '1' state (for example 0x40 value), and ***HIF_SMP0_RG*** register must be set to the 0x05 value.
- Example 5: Host PC software needs to access semaphore #2 of DPSEM area using dual-page DPRAM/DPSEM access mode via sub-page #0 (using ***HIF_SMP0_RG*** register). The corresponding

PC memory address will be (*BADDR3* + 0x8), and *HIF_SMP0_RG* register must be set to the 0xc0 value.

Since DPRAM/DPSEM area of *TORNADO-P62xx/P67* host PCI-bus interface is the memory mapped area, then host PC CPU and any other external PCI-bus master can use the following PCI-to-DPRAM/DPSEM data transfer techniques:

- *direct random access to variables and data arrays*, which are allocated anywhere within the DPRAM/DPSEM area
- *block data transfers* between PCI-bus master and DPRAM/DPSEM area using the PCI-bus mastering feature of active PCI-bus master
- *block data transfers under control of host PC DMA controller* between PCI-bus master and DPRAM/DPSEM area using memory-to-memory or memory-to-port transfer cycles.

Timeout control for PCI-to-DPRAM access for TORNADO-P62xx/P67 DSP systems

All accesses to *TORNADO-P62xx/P67* on-board DPRAM feature no arbitration delays for DSP and host PCI-bus interface unless both DSP and host PCI-bus interface are addressing the same DPRAM memory location. In the latter case there is no arbitration preferences, and the first accessing port will proceed without arbitration delay, whereas the other port will be pending until the first port will finish the access cycle. DPRAM access collision is resolved by means of DPRAM internal arbitration circuit.

TORNADO-P62xx/P67 DSP systems provides hardware timeout control for every PCI-to-DPRAM access in order to prevents host PCI-bus environment from infinite idling and crashing in case host PCI-bus interface is waiting for DPRAM access being granted within indefinite time period.

Timeout condition for PCI-to-DPRAM access occurs in case both host PCI-bus interface of *TORNADO-P62xx/P67* DSP systems and on-board DSP are addressing the same DPRAM memory location with the PCI-to-DPRAM access being activated during already active DSP-to-DPRAM access.

Hardware timeout control for every PCI-to-DPRAM access is set to 2 us. Once DPRAM access has not been granted during PCI-to-DPRAM access, then the *DPRAM_ERR* bit of *HIF_IS_RG* HIF register is set to the '1' state. This timeout condition will cancel current PCI-to-DPRAM access, and can generate the PCI-bus interrupt in case the *DPRAM_ERR_IE* of *HIF_IM_RG* is set to the '1' state and the *PCIC_INTCSR_RG* PCI operation register of AMCC S5933 PCIC is configured to generate interrupt on the AOB-to-PCI incoming mailbox #4 byte #3. Refer to the corresponding subsection later in this section for more details.

DPRAM_ERR bit of *HIF_IS_RG* HIF register can be cleared by host software by writing to the *HIF_CLR_DPRAM_ERR_RG* HIF register (data written will be ignored). Refer to the corresponding subsection below for more details.

CAUTION

There is no access collision in case DPSEM is accessed by both on-board TMS320C620x/C6701 DSP and host PCI-bus interface of *TORNADO-P62xx/P67* DSP systems.

DPRAM area of TORNADO-P64xx DSP systems

High-density DPRAM area of *TORNADO-P64xx* host PCI-bus interface is designed for communication between the host PCI-bus masters and on-board DSP environment via DPRAM memory.

CAUTION

TORNADO-P64xx DSP systems do not provide on-board DPSEM dual-port hardware semaphores for communication between host PC application and DSP application.

TORNADO-P64xx DSP systems normally provide direct mapping of all on-board 128Kx32 or 256Kx32 DPRAM to host PCI-bus 32-bit memory address space (above 1 Mbyte) and do not use memory paging method in order to access on-board DPRAM from host PC application as *TORNADO-P62xx/P67* DSP systems do.

Direct mapping of full *TORNADO-P64xx* on-board DPRAM memory into PCI-bus 32-bit memory address space delivers fast access from host PC application to any DPRAM location and allows simultaneous access to different DPRAM locations from different simultaneously running host 32-bit Windows applications.

CAUTION

Normal DPRAM area configuration of *TORNADO-P64xx* host PCI-bus interface with direct mapping of all on-board DPRAM to PCI-bus 32-bit memory space is supported by *TORNADO Software Development Kit* (*TSDK*) software for Windows only.

DPRAM area of *TORNADO-P64xx* host PCI-bus interface can be alternatively configured to appear as 32 kbyte sub-area of on-board DPRAM memory, which is allocated into PC UMB memory area (below 1 Mbyte) in order to provide compatibility with *TORNADO-P6x* DOS utilities/applications.

CAUTION

Alternative DPRAM area configuration of *TORNADO-P64xx* host PCI-bus interface with direct mapping of 32 kbyte sub-area of on-board DPRAM memory to PCI-bus UMB memory area (below 1 Mbyte) is supported by *TORNADO-P6x* DOS utilities only and is not supported by *TORNADO Software Development Kit* (*TSDK*) software for Windows.

CAUTION

Particular allocation and size of DPRAM area of *TORNADO-P64xx* host PCI-bus interface can be configured via supplied PC DOS utilities (*TP_DP1M.EXE* and *TP_DP32.EXE*).

CAUTION

The PCI-bus memory base address for DPRAM area is assigned by host PCI BIOS during PC boot procedure, and, if it is required, can be obtained by host PC application by reading AMCC S5933 PCIC on-chip BADDR-3 PCI-bus configuration register.

Host PC application does not normally need to read BADDR0..BADDR4 PCI-bus configuration registers of AMCC S5933 PCIC in order to get memory/IO base for particular PCI-bus area, since these PCI-bus configuration registers are automatically handled by *TORNADO-P6x* DOS utilities and *TORNADO Software Development Kit* (*TSDK*) software for Windows.

Due to direct mapping of full *TORNADO-P64xx* on-board DPRAM memory into PCI-bus 32-bit memory address space, *TORNADO-P64xx* DSP systems do not provide *HIF_SMP0_RG* and *HIF_SMP1_RG* HIF registers, which are available for *TORNADO-P62xx/P67* DSP systems only.

TORNADO-P64xx on-board DPRAM is always accessed without arbitration delays for both DSP and host PCI-bus interface, even in case both DSP and host PCI-bus interface are addressing the same DPRAM memory location.

CAUTION

Care must be taken by both host PC software and TMS320C64xx DSP software to ensure that they both are not writing simultaneously to the same DPRAM location.

CAUTION

Due to no arbitration delays during access to *TORNADO-P64xx* on-board DPRAM, *TORNADO-P64xx* DSP systems do not provide timeout control for PCI-to-DPRAM access, as it is available for *TORNADO-P62xx/P67* DSP systems, and therefore, there is no *DPRAM_ERR* bit of *HIF_IS_RG* HIF register and no *DPRAM_ERR_IE* of *HIF_IM_RG* HIF register available for *TORNADO-P64xx* DSP systems.

TORNADO-P64xx on-board DPRAM is a high-speed device and is accessed by host PCI-bus interface at maximum available 133 Mbyte/s PCI-bus speed using true 'PCI-bus burst cycles' without PCI-bus wait states. 'PCI burst transfers' to/from *TORNADO-P64xx* on-board DPRAM are automatically inserted by PCI-bus controller and handled by on-board hardware in case host PC application initializes bulk data transfers to/from on-board DPRAM.

Generating PCI-to-DSP and DSP-to-PCI interrupt requests via DPRAM

DPRAM area of host PCI-bus interface of *TORNADO-P62xx/P67* DSP systems and of *TORNADO-P64xx* DSP systems with 256Kx32 DPRAM provide *DPRAM_HM_RQ* and *DPRAM_MH_RQ* specific memory locations, which provide PCI-to-DSP and DSP-to-PCI interrupt generation along with standard DPRAM memory functionality.

DPRAM_HM_RQ and *DPRAM_MH_RQ* DSPRAM memory locations are allocated correspondingly at the DPRAM addresses 1FFFCH and 1FFF8H for 32Kx32 DPRAM of *TORNADO-P62xx/P67* DSP systems, at 3FFFCH and 3FFF8H DPRAM addresses for 64Kx32 DPRAM of *TORNADO-P62xx/P67* DSP systems, and at FFFFCH and FFFF8H relative DPRAM addresses (corresponding DSP addresses are 900FFFFCH and 900FFFF8H) for 256Kx32 DPRAM of *TORNADO-P64xx* DSP systems.

DPRAM_HM_RQ and *DPRAM_MH_RQ* DSPRAM memory locations can be used to generate PCI-to-DSP and DSP-to-PCI interrupt requests along with passing the 32-bit interrupt request code via these DPRAM memory locations. These memory locations are similar to mailboxes, which are used in AMCC S5933 PCIC controller, and deliver one more path of mutual interrupt generation between host PCI-bus and on-board DSP.

CAUTION

When host PCI-bus writes to the *DPRAM_HM_RQ* address, then active *DSP_DPRAM_IRQ* interrupt request is generated to the DSP environment. This interrupt request remains active until DSP will read contents of this DPRAM memory location. Writing to this DPRAM location from the DSP side does not effect the state of *DSP_DPRAM_IRQ* interrupt request.

CAUTION

When DSP writes to *DPRAM_MH_RQ* DPRAM address, then active *PCI_DPRAM_IRQ* interrupt request is generated to PCI-bus, which will remain active until host PCI-bus will read from this DPRAM memory location. Writing to *DPRAM_MH_RQ* DPRAM location from host PCI-bus side does not effect the state of *PCI_DPRAM_IRQ* interrupt request.

Once enabled via the HIF interrupt mask register, *PCI_DPRAM_IRQ* interrupt request can generate active PCI-bus interrupt request.

HIF/HPI Registers Area

HIF/HPI area of *TORNADO-P6x* host PCI-bus interface is designed for DSP/system control, communication between host PCI-bus masters and on-board DSP environment via mailboxes and interrupts, and for access to full TMS320C6x DSP environment via DSP on-chip HPI port.

HIF/HPI area of *TORNADO-P62/P67* host PCI-bus interface is mapped into 16-bit PCI-bus I/O area, whereas HIF/HPI area of *TORNADO-P6202/P6203/P64xx* host PCI-bus interface is mapped into 32-bit PCI-bus I/O area.

HIF/HPI area of *TORNADO-P6x* host PCI-bus interface can be accessed from either 32-bit Windows or 16-bit DOS host PC applications.

CAUTION

PCI-bus memory base address for HIF/HPI area is assigned by host PCI BIOS during PC boot procedure, and, if it is required, can be obtained by host application software by reading AMCC S5933 PCIC on-chip BADDR-4 PCI-bus configuration register.

Host PC application does not normally need to read BADDR0..BADDR4 PCI-bus configuration registers of AMCC S5933 PCIC in order to get memory/IO base for particular PCI-bus area, since these PCI-bus configuration registers are automatically handled by *TORNADO-P6x* DOS utilities and *TORNADO Software Development Kit* (*TSDK*) software for Windows.

Table 2-20 presents a register list for HIF/HPI area of *TORNADO-P6x* host PCI-bus interface.

Table 2-20. Register list of HIF/HPI area of host PCI-bus interface.

register name	register address	data format	access mode	PC reset value	description
HIF_SMP0_RG (TORNADO-P62xx/P67 only)	*BADDR4*+00H	D7..D0	r/w	0x00	DPRAM/DPSEL page selector #0 (refer to subsection "DPRAM/ DPSEM Area" for more details)
HIF_SMP1_RG (TORNADO-P62xx/P67 only)	*BADDR4*+04H	D7..D0	r/w	0x00	DPRAM/DPSEL page selector #1 (refer to subsection "DPRAM/ DPSEM area" for more details)
HIF_CONTROL_RG	*BADDR4*+08H	D7..D0	r/w	0x00	DSP Control register
HIF_IM_RG	*BADDR4*+10H	D7..D0	r/w	0x00	AOB-to-PCI interrupt mask register
HIF_IS_RG	*BADDR4*+14H	D7..D0	r	0x00	AOB-to-PCI interrupt status register

HIF_HM_RQ0_RG	*BADDR4*+18H	D7..D0	r/w	0x00	PCI-to-DSP request register #0
HIF_HM_RQ1_RG	*BADDR4*+1CH	D7..D0	r/w	0x00	PCI-to-DSP request register #1
HIF_CLR_DPRAM_ERR_RG (TORNADO-P62xx/P67 only)	*BADDR4*+20H	Data ignored	w	-	Clear DPRAM timeout error (write only, data is ignored)
HIF_CLR_HPI_ERR_RG	*BADDR4*+21H	Data ignored	w	-	Clear HPI timeout error (write only, data is ignored)
HIF_CLR_MH_RQ_RG	*BADDR4*+22H	Data ignored	w	-	Clear DSP-to-PCI request (write only, data is ignored)
HIF_DSP_BMODE_RG (TORNADO-P64xx only)	*BADDR4*+2CH	D7..D0	w	0x00	TMS320C64xx DSP bootmode control
***TORNADO-P62/P67* DSP on-chip 16-bit HPI port registers**					
HPI_HPIC_RG_LSW	*BADDR4*+30H	D15..D0	r/w	0x0008	HPI Control register (LSW)
HPI_HPIC_RG_MSW	*BADDR4*+32H	D15..D0	r/w	0x0008	HPI Control register (MSW)
HPI_HPIC_RG	*BADDR4*+30H	D31..D0	r/w	0x00080008	HPI Control register (32-bit alias)
HPI_HPIA_RG_LSW	*BADDR4*+34H	D15..D0	r/w	-	HPI Address register (LSW)
HPI_HPIA_RG_MSW	*BADDR4*+36H	D15..D0	r/w	-	HPI Address register (MSW)
HPI_HPIA_RG	*BADDR4*+34H	D31..D0	r/w	-	HPI Address register (32-bit alias)
HPI_HPID_AINC_RG_LSW	*BADDR4*+38H	D15..D0	r/w	-	HPI Data register with address autoincrement (LSW)
HPI_HPID_AINC_RG_MSW	*BADDR4*+3AH	D15..D0	r/w	-	HPI Data register with address autoincrement (MSW)
HPI_HPID_AINC_RG	*BADDR4*+38H	D31..D0	r/w	-	HPI Data register with address autoincrement (32-bit alias)
HPI_HPID_RG_LSW	*BADDR4*+3CH	D15..D0	r/w	-	HPI Data register (LSW)
HPI_HPID_RG_MSW	*BADDR4*+3EH	D15..D0	r/w	-	HPI Data register (MSW)
HPI_HPID_RG	*BADDR4*+3CH	D31..D0	r/w	-	HPI Data register (32-bit alias)

***TORNADO-P6202/P6203* DSP on-chip 32-bit Expansion Bus registers (asynchronous host port mode)**					
HPI32_HPID_RG	*BADDR4*+30H	D31..D0	r/w	-	32-bit expansion bus data register (XBD)
HPI32_HPIA_RG	*BADDR4*+34H	D31..D0	r/w	0x00000000	32-bit expansion bus slave address register (XBISA)
***TORNADO-P64xx* DSP on-chip 32-bit HPI port registers**					
HPI_HPIC_RG	*BADDR4*+30H	D31..D0	r/w	0x00080008	32-bit HPI Control register
HPI_HPIA_RG	*BADDR4*+34H	D31..D0	r/w	-	32-bit HPI Address register
HPI_HPID_AINC_RG	*BADDR4*+38H	D31..D0	r/w	-	32-bit HPI Data register with address autoincrement
HPI_HPID_RG	*BADDR4*+3CH	D31..D0	r/w	-	32-bit HPI Data register

Notes:
1. '*BADDR4*' denotes I/O base address of HIF/HPI area of host PCI-bus interface in accordance with table 2-16.
3. Register access modes: *r* - read only, *w* - write only, *r/w* - read/write.
4. '*LSW*' denotes Least Significant 16-bit Word; '*MSW*' denotes Most Significant 16-bit Word
5. Refer to original TI TMS320C6x documentation for details about TMS320C6x DSP HPI port and Expansion Bus.
6. All accesses to TMS320C6x DSP on-chip HPI registers and Expansion Bus registers shall be performed with the DSP being in the 'RUN' state. *TORNADO-P62/P67* DSP systems require that bit *HWOB* of HPI control register (HPIC) is set to the '1' state in order to meet LSW first data transmission.

HIF_CONTROL_RG HIF Register

HIF_CONTROL_RG HIF register of *TORNADO-P6x* host PCI-bus interface is designed for DSP reset control and for enable PCI-bus mastering from the DSP environment. Table 2-21 contains description of register bits for *HIF_CONTROL_RG* HIF register.

***HIF_CONTROL_RG register* (r/w)**

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
DSP_M_GO *(r)*	*DSP_PD* *(r)* *(TORNADO-P62xx/P67)* *0* *(TORNADO-P64xx)*	*0*	*AM_EN* *(r/w, 0+))*	*0*	*0*	*M_SA_MODE* *(r/w, 0+)*	*M_GO* *(r/w,0+)*

Table 2-21. Register bits of *HIF_CONTROL_RG* HIF register.

register bit	***access mode***	***PC reset value***	***Description***
M_GO	r/w	0	Controls reset signal for on-board DSP during DSP host mode (in case *M_SA_MODE* bit is set to the '0' state). *M_GO* =0 corresponds to the RESET state of on-board TMS320C6x DSP. *M_GO* =1 corresponds to the RUN state of on-board TMS320C6x DSP (i.e. the on-board DSP is in the program execution mode).
M_SA_MODE	r/w	0	Sets operation mode for on-board DSP (either host mode or stand-alone mode). For more details refer to section "TS320C6x DSP Environment" earlier in this chapter. *M_SA_MODE* =0 sets DSP host mode, i.e. DSP reset signal is controlled by host PCI-bus via *M_GO* bit of *HIF_CONTROL_RG* HIF register. *M_SA_MODE* =1 sets DSP stand-alone mode, i.e. DSP reset signal is controlled by on-board reset pushbutton (SW1), external DSP reset input via on-board JP7 connector, and WDT expiration event (if WDT is enabled via *DSP_WDT_EN_RG* IOX register).
AM_EN	r/w	0	Enable control for PCI-bus mastering from DSP environment. For more details refer to section "TMS320C6x DSP Environment" earlier in this chapter. *AM_EN* =0 disables PCI-bus mastering from DSP environment, i.e. on-board DSP is unable to set *AMW_EN* and *AMR_EN* bit of *DSP_AMWREN_RG* IOX register to the '1' state in order to initialize the DSP-to-PCI and PCI-to-DSP transfers using PCI-bus mastering. *AM_EN* =1 enables PCI-bus mastering from DSP environment, i.e. on-board DSP can set *AMW_EN* and *AMR_EN* bit of *DSP_AMWREN_RG* IOX register to the '1' state in order to initialize the DSP-to-PCI and PCI-to-DSP transfers using PCI-bus mastering.
DSP_PD (TORNADO-P62xx/P67 only)	r	0	DSP power down status for *TORNADO-P62xx/P67* on-board TMS320C620x/C6701 DSP (refer to original TI documentation for more details about TMS320C6x DSP power down modes). *DSP_PD*=0 indicates that on-board TMS320C620x/C6701 DSP is not in the power down either PD2 or PD3 state. *DSP_PD*=1 indicates that on-board TMS320C620x/C6701 DSP is either in the power down either PD2 or PD3 state.

DSP_M_GO	r	0	Returned state of the DSP reset signal. *DSP M_GO* bit can be used to get current status of DSP reset signal for DSP stand-alone mode, and allows to prevent host-to-HPI accesses timeouts while DSP is in the reset state. In case DSP operates in host mode (*M_SA_MODE* bit of *HIF_CONTROL_RG* register is set to the '0' state), then *DSP M_GO* bit is a returned copy of the *M_GO* bit. In case DSP operates in stand-alone mode (*M_SA_MODE* bit of *HIF_CONTROL_RG* register is set to the '1' state), then *DSP_M_GO* bit indicates current state of DSP reset signal, which might be controlled by on-board DSP reset pushbutton (SW1), external DSP reset input via on-board JP7 connector, and WDT expiration event (if WDT is enabled via *DSP_WDT_EN_RG* IOX register). *DSP_M_GO*=0 indicates that on-board TMS320C6x DSP is in the RESET state. *DSP_M_GO*=1 indicates that on-board TMS320C6x DSP is in the RUN state (program execution mode).

Note:
1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on PC reset condition.

Accessing DSP memory areas via DSP on-chip HPI port for TORNADO-P62/P67/P64xx DSP systems

Host PCI-bus interface of *TORNADO-P62/P67/P64xx* DSP systems supports PCI-to-DSP communication via TMS320C6201/C6701/C64xx DSP on-chip host-port interface (HPI). Along with *TORNADO-P62/P67/P64xx* on-board DPRAM memory area, TMS320C6201/C6701/C64xx DSP on-chip HPI port is another high-performance data path for communication between host PC application and DSP application via all DSP on-chip/off-chip memory areas.

TMS320C6201/C6701/C64xx DSP on-chip HPI control registers appear as a part of the HIF/HPI area of host PCI-bus interface of *TORNADO-P62/P67* DSP systems (table 2-20).

CAUTION

This manuals does not provide details about how to use TMS320C6201/C6701/C64xx DSP on-chip HPI port.

Refer to original TI documentation about details for TMS320C6201/C6701/C64xx DSP on-chip HPI port.

CAUTION

TORNADO-P62/P67 DSP systems with TMS320C6201/C6701 DSP provide DSP on-chip 16-bit HPI port.

HWOB bit of TMS320C6201/C6701 DSP *HPI_HPIC_RG* register must be set to the '1' state prior any access to *HPI_HPIA_RG*, *HPI_HPID_AINC_RG* and *HPI_HPID_RG* registers. This corresponds to 16-bit LSW first communication via host PCI-bus interface.

Host PCI-bus access to 32-bit *HPI_HPIC_RG*, *HPI_HPIA_RG*, *HPI_HPID_AINC_RG* and *HPI_HPID_RG* registers of *TORNADO-P62/P67* DSP systems can done using either 32-bit PCI-bus access cycles or two sequential 16-bit PCI-bus access cycles (LSW first and MSW last). Any violation of this access requirement may result in invalid data passed.

CAUTION

TORNADO-P64xx DSP systems with TMS320C64xx DSP are configured with DSP on-chip 32-bit HPI port.

HWOB bit of *HPI_HPIC_RG* register is ignored for TMS320C64xx DSP on-chip 32-bit HPI port of *TORNADO-P64xx* DSP systems.

Host PCI-bus access to 32-bit *HPI_HPIC_RG*, *HPI_HPIA_RG*, *HPI_HPID_AINC_RG* and *HPI_HPID_RG* registers of *TORNADO-P64xx* DSP systems can done using 32-bit PCI-bus access cycles only. Any violation of this access requirement may result in invalid data passed.

DSP on-chip HPI port of *TORNADO-P62/P67/P64xx* DSP systems also supports generation of DSP-to-PCI (*HPI_HINT*) and PCI-to-DSP (*HPI_DSPINT*) mutual interrupts. *HPI_HINT* DSP-to-PCI interrupt can be enabled via *HIF_IM_RG* HIF register and generate AOB-to-PCI interrupt.

CAUTION

TMS320C6201/C6701/C64xx DSP on-chip HPI port of *TORNADO-P62/P67/P64xx* DSP systems can operate only in case DSP is either in the 'RUN' state, otherwise HPI timeout error is set.

Accessing DSP memory areas via DSP expansion bus for TORNADO-P6202/P6203

Host PCI-bus interface of *TORNADO-P6202/P6203* DSP systems supports PCI-to-DSP communication via 32-bit expansion bus of TMS320C6202/TMS320C6203 DSP. Along with *TORNADO-P6202/P6203* on-board

DPRAM/DPSEM area, 32-bit expansion bus (in asynchronous host port mode) of TMS320C6202/TMS320C6203 DSP is another high-performance data path for communication between DSP and host PC via all DSP on-chip/off-chip memory areas.

CAUTION

TORNADO-P6202/P6203 DSP systems have been designed using asynchronous host port (HPI) mode of expansion bus of TMS320C6201/TMS320C6701 DSP, which appears identical to operation of DSP on-chip HPI port of *TORNADO-P62/P67* DSP systems except for minor differences.

32-bit DSP on-chip expansion bus control registers for asynchronous host port mode (XBD and XBISA, which are denoted as *HPI32_HPID_RG* and *HPI32_HPID_RG* in table 2-20) appear as a part of the HIF/HPI area of host PCI-bus interface of *TORNADO-P6202/P6203* DSP systems (table 2-20).

CAUTION

This manuals does not provide details about how to use asynchronous host port mode of TMS320C6202/C6203 DSP expansion bus.

Refer to original TI documentation about details on expansion bus operation for TMS320C6202/TMS320C6203 DSP.

CAUTION

Host PCI-bus access to *HPI32_HPIA_RG* and *HPI32_HPID_RG* registers of *TORNADO-P6202/P6203* DSP systems can done using 32-bit PCI-bus access cycles. Any violation of this access requirement may result in invalid data passed.

Asynchronous HPI port mode of 32-bit expansion bus of *TORNADO-P6202/P6203* on-board TMS320C6202/TMS320C6203 DSP also supports generation of PCI-to-DSP (*HPI_DSPINT*) interrupt.

CAUTION

Asynchronous HPI port mode of 32-bit expansion bus of *TORNADO-P6202/P6203* on-board TMS320C6202/TMS320C6203 DSP can does not support generation of DSP-to-PCI (*HPI_HINT*) interrupt.

HPI_HINT bit of *HIF_IS_RG* register and *HPI_HINT_IE* bit of *HIF_IM_RG* register are not available for *TORNADO-P6202/P6203* DSP systems.

CAUTION

Asynchronous HPI port mode of 32-bit expansion bus of *TORNADO-P6202/P6203* on-board TMS320C6202/TMS320C6203 DSP can operate only in case DSP is in the 'RUN' state, otherwise HPI timeout error is set.

Timeout Control for Host-to-HPI Access and for expansion bus access

In accordance with TMS320C6x DSP specifications, host-to-HPI access for *TORNADO-P62/P67/P64xx* DSP systems (hereafter HPI port of *TORNADO-P6x* DSP systems denotes both DSP on-chip HPI port of *TORNADO-P62/P67/P64xx* DSP systems and expansion bus in asynchronous host port mode of *TORNADO-P6202/P6203* on-board TMS320C6202/TMS320C6203 DSP) is allowed only in case DSP is in the RUN state (program execution mode), i.e. the DSP reset signal is released. Otherwise, in case HPI is accessed while DSP is either in the reset state or in the PD2/PD3 power-down state (*TORNADO-P62xx/P67* only), then HPI access results in DSP on-chip clock stopped and host-to-HPI access pending with the HPI ready (*HPI_READY*) hardware signal set to non-ready state until DSP is restarted. This might result in infinite host PCI-bus idling condition and further crashing of host PC environment. Normally, *HPI_READY* signal comes to the active state within several DSP clock cycles to confirm end of HPI data transfer.

In order to avoid infinite pending of host PCI-bus during host-to-HPI access, *TORNADO-P6x* host PCI-bus interface features hardware timeout control for host-to-HPI access. Timeout interval for host-to-HPI access is set to 2 μsec.

CAUTION

Once HPI timeout will occur, this will result in termination of currently active host-to-HPI access and setting *HPI_ERR* bit of *HIF_IS_RG* HIF register to the '1' state. *HPI_ERR*=1 condition can generate active AOB-to-PCI interrupt in case bit *HPI_ERR_IE* of *HIF_IM_RG* interrupt mask HIF register is set to the '1' state.

Host PCI-bus master can clear *HPI_ERR* bit by writing to *HIF_CLR_HPI_ERR_RG* write-only register with the written data ignored (refer to table 2-20).

Generation of PCI-bus interrupt

TORNADO-P6x provides generation of one PCI-bus interrupt request via AMCC S5933 PCIC. Host PCI-bus interrupt request is generated as the logical OR of the following individually masked sources:

- *from AMCC S5933 PCIC on-chip resources*, as defined by the corresponding bits of *HOST_PCIC_INTCSR_RG* AMCC S5933 PCIC on-chip PCI interrupt control/status operation register (refer to the corresponding subsection earlier in this section and to Appendix B):
  - in case any selected byte of outgoing mailbox (*HOST_PCIC_OMBXn_RG* AMCC S5933 PCIC on-chip PCI operation registers) goes empty
  - in case any selected byte of incoming mailbox (*HOST_PCIC_IMBXn_RG* AMCC S5933 PCIC on-chip PCI operation registers) becomes full (except for byte #3 of mailbox *HOST_PCIC_IMBX3_RG* incoming mailbox register)
  - in case DSP controlled PCI-bus mastering data transfer from the DSP environment completes
- *from TORNADO-P6x specific on-board resources*, which can be individually enabled via *HIF_IM_RG* interrupt mask HIF register and are ORed together in order to load byte #3 of *HOST_PCIC_IMBX3_RG* AMCC S5933 PCIC on-chip PCI incoming mailbox register (actual data of byte #3 must be ignored by host PC application):
  - in case of DPRAM host interrupt (*PCI_DPRAM_IRQ*) comes active and *PCI_DPRAM_IE* bit of *HIF_IM_RG* HIF register is set to the '1' state (*TORNADO-P62xx/P67* DSP systems and *TORNADO-P64xx* DSP systems with 256Kx32 DPRAM only)
  - in case DSP HPI-port interrupt (*HPI_HINT*) comes active and *HPI_HINT_IE* bit of *HIF_IM_RG* HIF register is set to the '1' state (*TORNADO-P62/P67/P64xx* DSP systems only)
  - in case DSP-to-PCI request (*MH_RQ*) is generated by DSP via *DSP_MH_RQ_RG* IOX register of DSP environment and *MH_RQ_IE* bit of *HIF_IM_RG* HIF register is set to the '1' state
  - in case of DPRAM access timeout condition (*DPRAM_ERR*) (*TORNADO-P62xx/P67* DSP systems and *TORNADO-P64xx* DSP systems with 256Kx32 DPRAM only) and *DPRAM_ERR_IE* bit of *HIF_IM_RG* HIF register is set to the '1' state
  - in case of HPI access timeout condition (*HPI_ERR*) and *HPI_ERR_IE* bit of *HIF_IM_RG* HIF register is set to the '1' state.

CAUTION

In order to enable PCI-bus interrupt request from *TORNADO-P6x* specific on-board resources, *HOST_PCIC_INTCSR_RG* AMCC S5933 PCIC on-chip PCI interrupt control/status operation register must be configured by host software to generate PCI-bus interrupt on load event for byte #3 of incoming mailbox #4.

Once PCI-bus interrupt request from *TORNADO-P6x* specific on-board resources is enabled, then AMCC S5933 PCIC will be not able to generate PCI-bus interrupt request on other PCI incoming mailbox condition.

CAUTION

PCI-bus interrupt request number, which is allocated to *TORNADO-P6x* DSP system, is assigned by host PCI BIOS during PC boot procedure, and can be obtained by host software by reading the AMCC S5933 PCIC on-chip *INTLN* PCI configuration register (offset 3CH).

Refer to Appendix B of this manual and original documentation for AMCC S5933 PCIC for more details about programming AMCC S5933 PCIC.

HIF_IS_RG interrupt status and HIF_IM_RG interrupt mask registers

Current state of *TORNADO-P6x* specific on-board interrupt request sources can be obtained via *HIF_IS_RG* interrupt status HIF register:

***HIF_IS_RG register* (r/w)**

Bit-7	Bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	Bit-0
0	*0*	*HPI_ERR (r)*	*DPRAM_ERR (r) (TORNADO-P62xx/P67)*	*0*	*MH_RQ (r)*	*HPI_HINT (r) (TORNADO-P62/P67/P64xx)* *0 (TORNADO-P6202/P6203)*	*PCI_DPRAM_IRQ (r) (TORNADO-P62xx/P67 and TONRADO-P64xx with 256Kx32 DPRAM)* *0 (TONRADO-P64xx with 128Kx32 DPRAM)*

HIF_IM_RG HIF register of *TORNADO-P6x* host PCI-bus interface must be used to enable *TORNADO-P6x* specific on-board host interrupt sources, which can generate PCI-bus interrupt via byte #3 of incoming mailbox #4 of AMCC S5933 PCIC (refer to subsection “Generation of PCI-bus Interrupt” earlier in this section):

***HIF_IM_RG register* (r/w)**

bit-7	bit-6	Bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	*0*	*HPI_ERR_IE (r/w, 0+)*	*DPRAM_ERR_IE (r/w, 0+) (TORNADO-P62xx/P67)*	*0*	*MH_RQ_IE (r/w, 0+)*	*HPI_HINT_IE (r/w, 0+) (TORNADO-P62/P67/P64xx)* *0 (TORNADO-P6202/P6203)*	*PCI_DPRAM_IRQ_IE (r/w,0+) (TORNADO-P62xx/P67 and TONRADO-P64xx with 256Kx32 DPRAM)* *0 (TONRADO-P64xx with 128Kx32 DPRAM)*

CAUTION

The '1' state for interrupt enable bits of *HIF_IM_RG* Interrupt Mask HIF register of *TORNADO-P6x* host PCI-bus interface enables the corresponding *TORNADO-P6x* specific host interrupt source, and generates byte #3 load event for DSP-to-PCI incoming mailbox #4 of S5933 PCIC.

The '0'state for interrupt enable bits of *HIF_IM_RG* HIF register of *TORNADO-P6x* host PCI-bus interface disables the corresponding *TORNADO-P6x* specific host interrupt source. All *TORNADO-P6x* specific host interrupt sources are disabled on host PC reset condition.

Tables 2-22 and 2-23 contain description for register bits of *HIF_IM_RG* interrupt mask and *HIF_IS_RG* interrupt status registers.

Table 2-22. Register bits of *HIF_IS_RG* register.

register bits	access mode	Value on PC reset	Description
PCI_DPRAM_IRQ *(TORNADO-P62xx/P67 and TORNADO-P64xx with 256Kx32 DPRAM)*	r	-	Status of DSP-to-PCI interrupt request via DPRAM (*TORNADO-P62xx/P67* DSP systems and *TORNADO-P64xx* DSP systems with 256Kx32 DPRAM only). For more details refer to section "TMS320C6x DSP Environment" earlier in this chapter. *PCI_DPRAM_IRQ* =0 denotes that there is no active DSP-to-PCI interrupt request via DPRAM. *PCI_DPRAM_IRQ* =1 denotes that there is active DSP-to-PCI interrupt request via DPRAM, i.e. on-board DSP has written to *DPRAM_MH_RQ* DPRAM memory location (address 1FFF8H for *TORNADO-P62xx/P67* with 32Kx32 DPRAM, address 3FFF8H for *TORNADO-P62xx/P67* with 64Kx32 DPRAM, and address 900FFFF8H for *TORNADO-P64xx* with 256Kx32 DPRAM). *PCI_DPRAM_IRQ* interrupt request will remain active until host PCI-bus master reads from the *DPRAM_MH_RQ* memory location.

HPI_HINT *(TORNADO-P62/P67/P64xx)*	r	0	Status of DSP-to-PCI interrupt request via DSP on-chip HPI port (*TORNADO-P62/P67/P64xx* DSP systems only). For more details refer to section "TMS320C6x DSP Environment" earlier in this chapter and to original TI TMS320C6x DSP documentation. *HPI_HINT* =0 denotes that there is no active DSP-to-PCI interrupt request via DSP on-chip HPI port. *HPI_HINT* =1 denotes that there is active DSP-to-PCI interrupt request via DSP on-chip HPI port, i.e. on-board DSP has set HINT bit of DSP on-chip HPIC register to the '1' state. *HPI_HINT* interrupt request will remain active until host PCI-bus master clears HINT bit of DSP on-chip HPIC register.
MH_RQ	r	0	Status of DSP-to-PCI interrupt request via *DSP_MH_RQ_RG* IOX register. For more details refer to section "TMS320C6x DSP Environment" earlier in this chapter. *MH_RQ* =0 denotes that there is no active DSP-to-PCI interrupt request via *DSP_MH_RQ_RG* IOX register. *MH_RQ* =1 denotes that there is active DSP-to-PCI interrupt request via *DSP_MH_RQ_RG* IOX register, i.e. on-board DSP has written to the *DSP_MH_RQ_RG* IOX register. *MH_RQ* interrupt request will remain active until host PCI-bus master will clear *MH_RQ* by writing to the *HIF_CLR_MH_RQ_RG* write-only HIF register (written data is ignored).
DPRAM_ERR *(TORNADO-P62xx/P67*	r	0	Status of DPRAM access timeout error for PCI-to-DPRAM access (*TORNADO-P62xx/P67* only). For more details refer to the corresponding subsection above. *DPRAM_ERR* =0 denotes that no DPRAM timeout event has been detected during PCI-to-DPRAM access. *DPRAM_ERR* =1 denotes that DPRAM timeout event has been detected during PCI-to-DPRAM access. *DPRAM_ERR* interrupt request will remain active until host PCI-bus master will clear *DPRAM_ERR* by writing to the *HIF_CLR_DPRAM_ERR_RG* write-only HIF register (written data is ignored).
HPI_ERR	r	0	Status of HPI access timeout error for PCI-to-HPI access. For more details refer to the corresponding subsection above. *HPI_ERR* =0 denotes that no HPI timeout event has been detected during PCI-to-HPI access. *HPI_ERR* =1 denotes that HPI timeout event has been detected during PCI-to-DPRAM access. *HPI_ERR* interrupt request will remain active until host PCI-bus master will clear *HPI_ERR* by writing to the *HIF_CLR_HPI_ERR_RG* write-only HIF register (written data is ignored).

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on PC reset condition.

Table 2-23. Register bits of *HIF_IM_RG* register.

register bits	access mode	Value on PC reset	Description
PCI_DPRAM_IE *(TORNADO-P62xx/P67 and TORNADO-P64xx with 256Kx32 DPRAM)*	r	0	Enable mask for generation of host PCI-bus interrupt request on DSP-to-PCI interrupt request via DPRAM (*TORNADO-P62xx/P67* DSP systems and *TORNADO-P64xx* DSP systems with 256Kx32 DPRAM only). For more details refer to section "TMS320C6x DSP Environment" earlier in this chapter. *PCI_DPRAM_IE* =0 disables generation of host PCI-bus interrupt request on active DSP-to-PCI interrupt request via DPRAM. *PCI_DPRAM_IE* =1 enables generation of host PCI-bus interrupt request on active DSP-to-PCI interrupt request via DPRAM.
HPI_HINT_IE *(TORNADO-P62/P67/P64xx)*	r	0	Enable mask for generation of host PCI-bus interrupt request on DSP-to-PCI interrupt request via DSP on-chip HPI port (*TORNADO-P62/P67/P64xx* DSP systems only). For more details refer to original TI TMS320C6x DSP documentation. *HPI_HINT_IE* =0 disables generation of host PCI-bus interrupt on active DSP-to-PCI interrupt request via DSP on-chip HPI port. *HPI_HINT_IE* =1 enables generation of host PCI-bus interrupt on active DSP-to-PCI interrupt request via DSP on-chip HPI port.
MH_RQ_IE	r	0	Enable mask for generation of host PCI-bus interrupt request on DSP-to-PCI interrupt request via *DSP_MH_RQ_RG* IOX register. For more details refer to section "TMS320C6x DSP Environment" earlier in this chapter. *MH_RQ_IE* =0 disables generation of host PCI-bus interrupt on active DSP-to-PCI interrupt request via *DSP_MH_RQ_RG* IOX register. *MH_RQ_IE* =1 enables generation of host PCI-bus interrupt on active DSP-to-PCI interrupt request via *DSP_MH_RQ_RG* IOX register.
DPRAM_ERR_IE *(TORNADO-P62xx/P67*	r	0	Enable mask for generation of host PCI-bus interrupt request on DPRAM access timeout error for PCI-to-DPRAM access (*TORNADO-P62xx/P67* only). For more details refer to the corresponding subsection above. *DPRAM_ERR_IE* =0 disables generation of host PCI-bus interrupt on DPRAM access timeout error. *DPRAM_ERR_IE* =1 enables generation of host PCI-bus interrupt on DPRAM access timeout error.

HPI_ERR_IE	r	0	Enable mask for generation of host PCI-bus interrupt request on HPI access timeout error for PCI-to-HPI access. For more details refer to the corresponding subsection above. *HPI_ERR_IE* =0 disables generation of host PCI-bus interrupt on HPI access timeout error. *HPI_ERR_IE* =1 enables generation of host PCI-bus interrupt on HPI access timeout error.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on PC reset condition.

HIF_HM_RQ0_RG and HIF_HM_RQ1_RG registers for generation PCI-to-DSP interrupt requests

HIF_HM_RQ0_RG and *HIF_HM_RQ1_RG* HIF registers are used to generation of PCI-to-DSP interrupt and to pass 4-bit token (bits D3..D0).

***HIF_HM_RQ0_RG register* (r/w)**
***HIF_HM_RQ1_RG register* (r/w)**

x	*0*	*0*	*0*	*0*	*D3 (r/w, 0+)*	*D2 (r/w, 0+)*	*D1 (r/w, 0+)*	*D0 (r/w, 0+)*
bit-31...bit-8	bit-7	bit-6	bit-5	bit-4	Bit-3	bit-2	bit-1	bit-0

Contents of *HIF_HM_RQ0_RG* and *HIF_HM_RQ1_RG* HIF registers are available for read-only and reset-only by on-board DSP via *DSP_HM_RQ0_RG* and *DSP_HM_RQ1_RG* read-only IOX registers (refer to section "TMS320C6x DSP Environment" earlier in this chapter).

In case host PCI-bus master writes to *HIF_HM_RQ0_RG* register, then this event generate active *HM_RQ0* PCI-to-DSP request, which can generate active DSP interrupt request in case any of DSP external interrupt selector registers is configured for DSP interrupt on *HM_RQ0* event. Similarly, In case host PCI-bus master writes to *HIF_HM_RQ1_RG* register, then this event generate active *HM_RQ1* PCI-to-DSP request, which can generate active DSP interrupt request in case any of DSP external interrupt selector registers is configured for DSP interrupt on *HM_RQ1* event.

The 4-bit token, which is passed via *HIF_HM_RQ0_RG* and *HIF_HM_RQ1_RG* HIF registers from host PCI-bus master, can be used by the DSP software to identify interrupt specific information. After DSP has read and decoded the contents of *DSP_HM_RQ0_RG* and *DSP_HM_RQ1_RG* IOX registers, it can clear these registers in order to confirm to host PCI-bus master that interrupt request has been processed (the requesting host PCI-bus master can perform periodical polling of contents of *HIF_HM_RQ0_RG* and *HIF_HM_RQ1_RG* read/write registers).

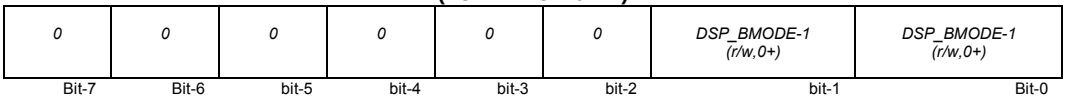
HIF_HM_RQ0_RG and *HIF_HM_RQ1_RG* HIF registers actually function as 4-bit PCI-to-DSP outgoing mailbox registers, and are similar to 32-bit PCI-to-DSP outgoing mailbox registers *PCIC_OMBXx_RG* of the S5933 PCIC. However, despite S5933 PCIC PCI-to-DSP outgoing mailboxes, DSP can clear the contents of *HIF_HM_RQ0_RG* and *HIF_HM_RQ1_RG* HIF registers after generated DSP request has been processed, furthermore, each of *HIF_HM_RQ0_RG* and *HIF_HM_RQ1_RG* HIF registers can generate individual interrupt request to on-board DSP. The latter feature adds two independent interrupt request paths into PCI-to-DSP interrupt communication along with the *DSP_DPRAM_IRQ* interrupt via DPRAM and the AOB interrupt request from S5933 PCIC. *HIF_HM_RQ0_RG* and *HIF_HM_RQ1_RG* HIF registers allow two external PCI-

bus masters to generate two independent PCI-to-DSP interrupt requests to *TORNADO-P6x* on-board DSP, that simplifies DSP interrupt decoding software and reduces interrupt processing times.

HIF_DSP_BMODE_RG register for DSP bootmode control for TORNADO-P64xx DSP systems

TORNADO-P64xx DSP systems allow to configure TMS320C64xx DSP bootmode from host PC application in accordance with table 2-2b in case DSP is running in *host PC operation mode* via *HIF_DSP_BMODE_RG* HIF register of host PCI-bus interface. Also, *HIF_DSP_BMODE_RG* HIF register of host PCI-bus interface can be used by host PC application anytime to read current bootmode configuration for *TORNADO-P64xx* on-board DSP. Refer to table 2-2b and section "TMS320C6x DSP Environment" earlier in this chapter for more details.

***HIF_DSP_BMODE_RG register* (r/w)**
(*TORNADO-P64xx*)



CAUTION

Write to {*DSP_BMODE-1, DSP_BMODE-0*} bits of *HIF_DSP_BMODE_RG* HIF register of *TORNADO-P64xx* host PCI-bus interface has effect only in case on-board DSP is running in *host PC operation mode* (in case *TORNADO-P64xx* board is installed into host PCI-bus slot and *M_SA_MODE* bit of *HIF_CONTROL_RG* register of host PCI-bus interface is set to the '0' state) while DSP is in the 'RESET' state (*M_GO* bit of *HIF_CONTROL_RG* HIF register is in the '0' state).

{*DSP_BMODE-1, DSP_BMODE-0*} bits of *HIF_DSP_BMODE_RG* HIF register of *TORNADO-P64xx* host PCI-bus interface are read-only in case on-board TMS320C64xx DSP is running in *host PC operation mode* while DSP is in the 'RUN' state, and can be used to read DSP bootmode configuration, which has been latched on last release of DSP reset signal.

{*DSP_BMODE-1, DSP_BMODE-0*} bits of *HIF_DSP_BMODE_RG* HIF register of *TORNADO-P64xx* host PCI-bus interface are read-only in case on-board TMS320C64xx DSP is running in *stand-alone operation mode* (in case either *TORNADO-P64xx* board is either not installed into host PCI-bus slot, or in case *TORNADO-P64xx* board is installed into host PCI-bus slot and *M_SA_MODE* bit of *HIF_CONTROL_RG* register of host PCI-bus interface is set to the '1' state), and can be used to read current DSP bootmode configuration, which corresponds to on-board SW2-1/2 switch setting latched on last release of DSP reset signal.

Table 2-24 provides description for register bits of *HIF_DSP_BMODE_RG* register for *TORNADO-P64xx* DSP systems.

Table 2-24. Register bits of *HIF_DSP_BMODE_RG* register for *TORNADO-P64xx* DSP systems.

register bits	access mode	Value on PC reset	Description
{*DSP_BMODE-1, DSP_BMOE-0*}	r/w	[0,0]	Set bootmode configuration for *TORNADO-P64xx* on-board TMS320C64xx DSP in case DSP is running in host PC operation mode while DSP is in the 'RESET' state, and return current (last latched) DSP bootmode configuration for *TORNADO-P64xx* on-board DSP anytime for DSP host PC and stand-alone operation modes. Refer to table 2-2b and section "TMS320C6x DSP Environment" for more details about DSP bootmode configurations for *TORNADO-P64xx* DSP systems. {*DSP_BMODE-1, DSP_BMODE-0*} =[0,0] corresponds to '*NO BOOT*' DSP bootmode. {*DSP_BMODE-1, DSP_BMODE-0*} =[0,1] corresponds to '*HPI BOOT*' DSP bootmode. {*DSP_BMODE-1, DSP_BMODE-0*} =[1,0] corresponds to '*FLASH BOOT*' DSP bootmode. {*DSP_BMODE-1, DSP_BMODE-0*} =[1,1] is reserved.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on PC reset condition.

2.4 Parallel I/O Expansion DCM Site (PIOX/PIOX-16)

TORNADO-P6x system architecture allows to expand on-board I/O resources and DSP on-chip I/O resources via universal 16-/32-bit parallel I/O expansion (PIOX/PIOX-16) DCM site (JP1 at fig.2-2 and fig.A-1), which has been designed for installation of compatible either 32-bit PIOX or 16-bit PIOX-16 DCM.

PIOX/PIOX-16 DCM site is common for all *TORNADO* PC plug-in DSP systems and *TORNADO-E* embedded DSP controllers. A variety of 'off-the-shelf' PIOX/PIOX-16 DCM comprises of high-speed AD/DA/DIO and application specific I/O Coprocessor DCM for telecommunication, industrial and instrumentation, and many more applications.

Description

Parallel data bus of PIOX/PIOX-16 DCM site interface is directly accessed by *TORNADO-P6x* on-board TMS320C6x DSP.

32-bit PIOX DCM site interface area occupies 512Kx32 sub-area of TORNADO-P6x DSP memory map and is allocated into the corresponding sub-area of asynchronous EMIF CE-0 area of on-board TMS320C620x/C6701 DSP for *TORNADO-P62xx/P67* DSP systems (table 2-1a) and into EMIF-B CE-3 area of on-board TMS320C64xx DSP for *TORNADO-P64xx* DSP systems (table 2-1b).

16-bit PIOX-16 DCM site interface occupies least significant 16-bit word of 32-bit PIOX DCM site interface datawords within lowest 64Kx32 sub-area of PIOX DCM site memory map.

PIOX/PIOX-16 DCM site includes DSP data/address buses, control signals, TMS320C6x DSP on-chip timers I/O pins and external interrupt inputs, dedicated PIOX/PIOX-16 reset signal, and power supply lines. PIOX DCM site supports 32-bit data bus and 8/16/32-bit data transfer cycles, whereas PIOX-16 DCM site supports 16-bit data transfer cycles only.

Installation of PIOX/PIOX-16 DCM onto TORNADO-P6x Mainboard

Figure 2-9 shows installation of 32-bit PIOX DCM and 16-bit PIOX-16 DCM onto *TORNADO-P6x* mainboard.

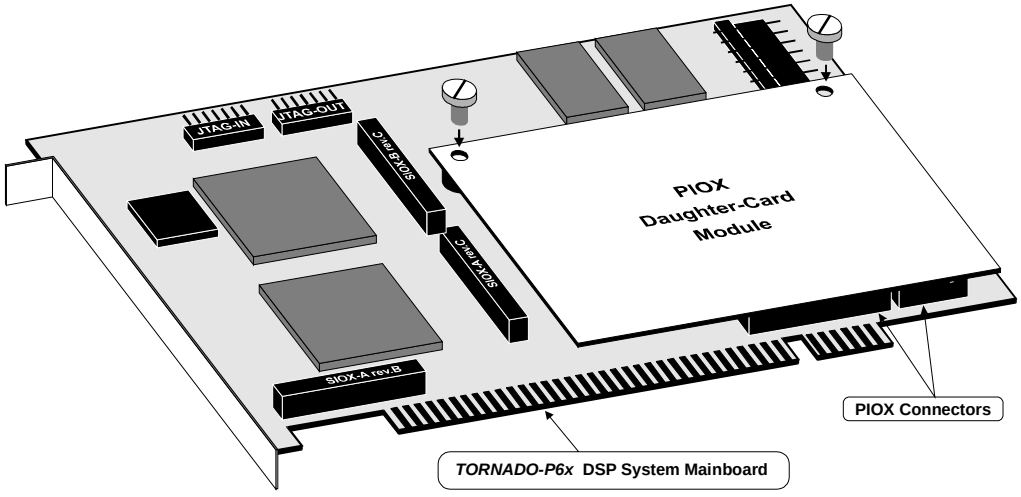


Fig.2-9a. Installation of 32-bit PIOX DCM onto *TORNADO-P6x* mainboard.

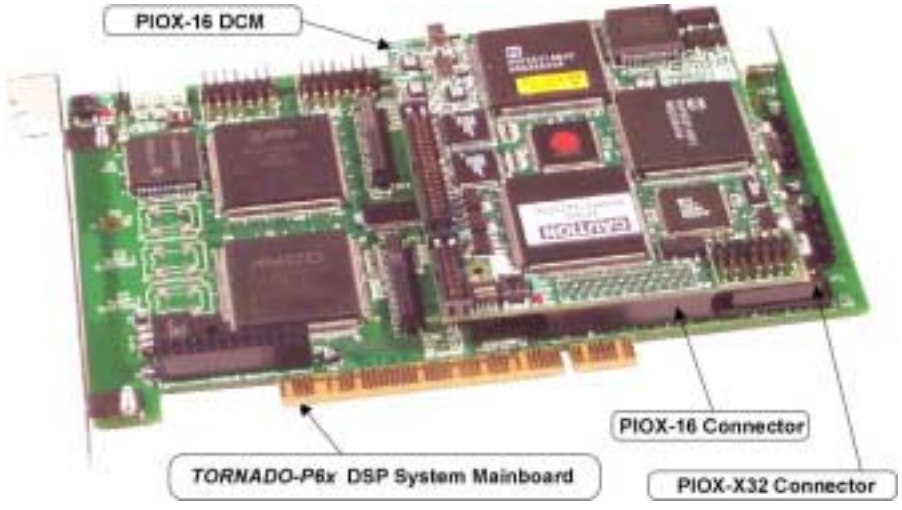


Fig.2-9b. Installation of 16-bit PIOX-16 DCM onto *TORNADO-P6x* mainboard.

Accessing PIOX/PIOX-16 DCM site interface from TMS320C6x DSP software

Parallel data bus of PIOX/PIOX-16 DCM site interface is directly accessed by *TORNADO-P6x* on-board TMS320C6x DSP in accordance with DSP memory map provided in tables 2-1a and 2-1b.

TORNADO-P62xx/P67 DSP systems provide direct connection of 32-bit parallel data bus of on-board PIOX/PIOX-16 DCM site interface to 32-bit EMIF data bus of on-board TMS320C620x/C6701 DSP. Therefore, any byte, 16-bit dataword, or full 32-bit data word of PIOX/PIOX-16 DCM site interface area can be accessed by *TORNADO-P62xx/P67* on-board DSP within one EMIF cycle as it is required by DSP application.

TORNADO-P64xx DSP systems provide connection of 32-bit parallel data bus of on-board PIOX/PIOX-16 DCM site interface to 16-bit EMIF-B data bus of on-board TMS320C64xx DSP. Therefore, any byte or 16-bit dataword of 32-bit dataword of PIOX/PIOX-16 DCM site interface area can be accessed by *TORNADO-P64xx* on-board DSP within one EMIF-B cycle as it is required by DSP application, whereas access to full 32-bit dataword of PIOX/PIOX-16 DCM site interface area will require two EMIF-B cycles for on-board TMS320C64xx DSP. *TORNADO-P64xx* DSP systems provide flexible configuration of data format for access to on-board PIOX/PIOX-16 DCM site interface area via {*PX_FMT-1,PX_FMT-0*} bits of *DSP_XIO_FMT_RG* IOX register. For more details refer to table 2-8 and subsection “Selection of data format for access to PIOX/PIOX-16 DCM site of *TORNADO-P64xx* DSP systems” of section “TMS320C6x DSP Environment” earlier in this chapter.

PIOX/PIOX-16 DCM site connector pinout

TORNADO-P6x on-board PIOX/PIOX-16 DCM site interface connector comprises of 16-bit PIOX-16 interface connector and PIOX-X32 32-bit add-on interface connector. This allows accommodation of either 16-bit PIOX-16 DCM or 32-bit PIOX DCM using one PIOX/PIOX-16 DCM site area.

Basic PIOX-16 16-bit interface connector p/n is DHB-RB50-S13NN, which is a high-density 50-pin DHB-series dual-row female connector with 0.05” pin pitch from Fujikura-DDK Ltd (www.ddkconnectors.com). Compatible PIOX-16 plug is DHB-PK50-S13NN, which is available upon request from MicroLAB Systems for design custom 16-bi PIOX-16 DCM.

PIOX-X32 add-on 32-bit interface connector p/n is DHB-RB30-S13NN, which is a high-density 30-pin DHB-series dual-row female connector with 0.05” pin pitch from Fujikura-DDK Ltd (www.ddkconnectors.com). Compatible PIOX-X32 plug is DHB-PK30-S13NN, which is available upon request from MicroLAB Systems for design custom 32-bit PIOX DCM.

PIOX/PIOX-16 connector pinout specification is presented at fig 2-10 and signal descriptions are provided in tables 2-25a and 2-25b.

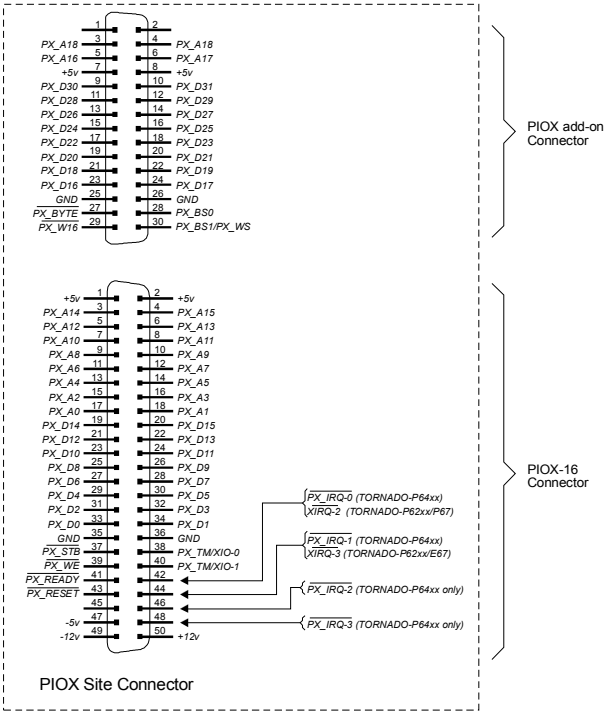


Fig.2-10. PIOX/PIOX-16 connector pinout (top view).

Table 2-25a. Signal description for PIOX-16 16-bit interface connector.

Signal name	signal type	description
PX_A[0..15]	O	16-bit LSW of PIOX/PIOX-16 address bus.
PX_D[0..15]	I/O	Buffered 16-bit LSW of PIOX/PIOX-16 data bus, which holds written data valid until next PIOX/PIOX-16 write cycle.
$\overline{PX\_STB}$	O	Active low PIOX/PIOX-16 data transfer strobe.
$\overline{PX\_WE}$	O	Active low PIOX/PIOX-16 write enable signal.
$\overline{PX\_READY}$	I	Active low pulled-up PIOX/PIOX-16 data ready acknowledge signal. It must be generated by installed PIOX/PIOX-16 DCM in order to terminate current PIOX/PIOX-16 data transfer cycle in accordance with the timing requirements for PIOX/PIOX-16 interface.

PX_TM/XIO-0 *PX_TM/XIO-1*	I/O/Z	Timer or I/O pins, which are connected to the corresponding TMS320C6x DSP on-chip timer I/O pins (TOUT0/TINP0 and TOUT1/TINP1). Each of these pins can be used as timer input, timer output, or general purpose I/O pin. Refer to figures 2-4a, 2-4b and 2-4c and section "TMS320C6x DSP Environment" earlier in this chapter for more details.
$\overline{PX\_RESET}$	O	Active low reset signal for the PIOX/PIOX-16 site, which is output of the *PX_RESET* bit of *DSP_PXSX_RESET_RG* IOX register (refer to table 2-11 and section "TMS320C6x DSP Environment" earlier in this chapter for more details).
$\overline{XIRQ-2}$ $\overline{XIRQ-3}$ *(TORNADO-P62x/P67)* *or* $\overline{PX\_IRQ-0}$, $\overline{PX\_IRQ-1}$ $\overline{PX\_IRQ-2}$ $\overline{PX\_IRQ-3}$ *(TORNADO-P64xx)*	I	Active low pulled-up interrupt request inputs from PIOX/PIOX-16 DCM site, which can be routed to external interrupt request inputs for on-board TMS320C6x DSP using DSP external interrupt selector registers (*DSP_EXT_INT4_SEL_RG.. DSP_EXT_INT7_SEL_RG* and *DSP_NMI_SEL_RG* IOX registers). Refer to table 2-12 and section "TMS320C6x DSP Environment" for more details. *TORNADO-P62xx/P67* DSP systems provide two PIOX/PIOX-16 interrupt request inputs ($\overline{XIRQ-2}$ and $\overline{XIRQ-3}$) with the $\overline{XIRQ-2}$ interrupt request input, which are shared with the corresponding interrupt request input of on-board SIOX rev.B DCM site. *TORNADO-P64xx* DSP systems provide four dedicated PIOX/PIOX-16 interrupt request inputs ($\overline{PX\_IRQ-0}$, $\overline{PX\_IRQ-1}$, $\overline{PX\_IRQ-2}$ and $\overline{PX\_IRQ-3}$), which are not shared with interrupt request inputs from on-board SIOX rev.B/C DCM sites.
GND		Ground.
+5v		+5v power (from PCI-bus or external power connector JP10).
+12v		+12v power (from PCI-bus or external power connector JP10).
-5v		-5v power (from on-board voltage regulator sourced from –12v on-board power).
-12v		-12v power (from PCI-bus or external power connector JP10).

Note:
1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
2. All logic I/O signal levels and load currents correspond to that for 3v/5v TTL logic.

Table 2-25b. Signal description for PIOX-X32 32-bit add-on interface connector.

Signal name	signal type	description
PX_A[16..18]	O	Extended PIOX address bus.
PX_D[16..31]	I/O	Buffered 16-bit MSW of PIOX data bus, which keeps written data valid until next PIOX/PIOX-16 write cycle.
$\overline{PX\_BYTE}$	O	Active low 8-bit (byte) data transfer cycle indicator. Byte selection signals *PX_BS0/BS1* define actual byte #0..#3 (byte #0 is LSB) inside 32-bit PIOX data word, which will be selected during PIOX data transfer cycle.

PX_W16	O	Active low 16-bit (halfword) data transfer cycle selector. 16-bit halfword selection signal *PX_WS* define actual 16-bit halfword #0/#1 (halfword #0 is LSW) inside 32-bit PIOX data word, which will be selected during PIOX data transfer cycle.
PX_BS0	O	Least significant bit of byte selection signals (*PX_BS0*, *PX_BS1*) for selection of particular byte during 8-bit (byte) data transfer cycle.
PX_BS1/PX_WS	O	Most significant bit of byte selection signals (*PX_BS0*, *PX_BS1*) for selection of particular byte during 8-bit (byte) data transfer cycle, and selector of particular 16-bit halfword selection signal (*WS*) for 16-bit data transfer cycle.
GND	-	Ground.
+5v	-	+5v power (from PCI-bus).

Note:
1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
2. All logic I/O signal levels and load currents correspond to that for 3v/5v TTL logic.

PIOX Data Transfer Cycles

PIOX DCM site interface of *TORNADO-P6x* supports 8-/16-/32-bit PIOX data access cycles. Particular type PIOX data access cycle is defined by $\overline{BYTE}$ and $\overline{W16}$ PIOX signals as the following:

- {$\overline{PX\_BYTE}$ =0, $\overline{PX\_W16}$ =1} state corresponds to *byte (8-bit) PIOX data transfer cycle*. Selection of particular byte (#0..#3) within addressed 32-bit data word id performed by (*PX_BS0*, *PX_BS1*) byte selection signals.
- {$\overline{PX\_BYTE}$ =1, $\overline{PX\_W16}$ =0} state corresponds to *16-bit half-word PIOX data transfer cycle*. Selection of particular 16-bit half-word (#0..#1) within addressed 32-bit data word id performed by *PX_BS1/PX_WS* signals. Signal *PX_BS0* is ignored.
- {$\overline{PX\_BYTE}$ =1, $\overline{PX\_W16}$ =1} state corresponds to *32-bit word PIOX data transfer cycle*. *PX_BS0* and *PX_BS1/PX_WS* signals are ignored in this mode.
- {$\overline{PX\_BYTE}$ =0, $\overline{PX\_W16}$ =0} state is reserved.

PIOX-16 Data Transfer Cycles

PIOX-16 connector does not contain the cycle definition signals, so PIOX-16 DCM site interface supports 16-bit data transfer cycles only.

Data Transfer Timing for PIOX/PIOX-16

PIOX/PIOX-16 data transfer timing diagram is presented at fig.2-11. This data transfer timing is known as the industry standard MOTO mode and assumes usage of data strobe signal and write enable signal.

CAUTION

Data transfer acknowledgement is provided by installed PIOX/PIOX-16 DCM by means of asynchronous *PX_READY* signal.

In case TMS320C6x DSP performs access to PIOX/PIOX-16 DCM site interface while PIOX/PIOX-16 DCM is not installed, then this results in missing *PX_READY* signal and infinite wait condition for *TORNADO-P6x* on-board TMS320C6x DSP.

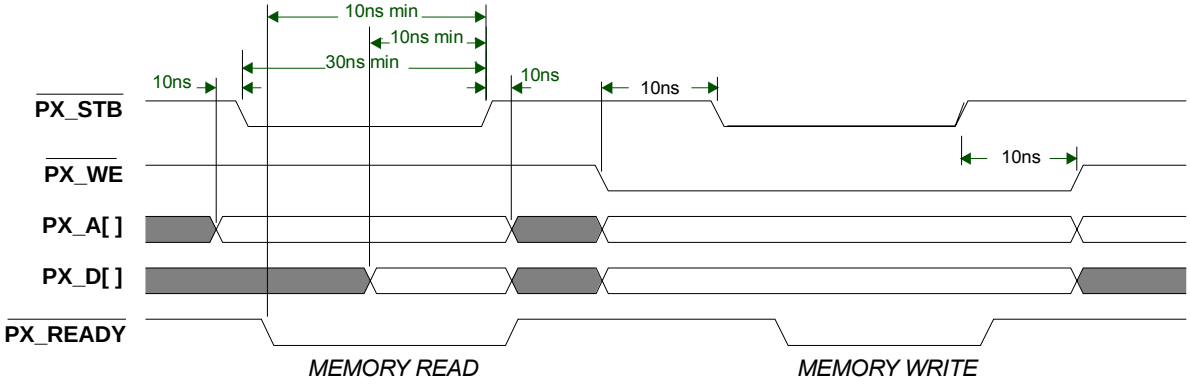


Fig.2-11. Timing diagram of PIOX/PIOX-16 data transfer strobe.

CAUTION

Minimum time duration for parallel data transfer strobe of PIOX/PIOX-16 DCM site interface must be 25ns (30ns is recommended) with setup/hold times 10ns. Data transfer acknowledgement is performed by means of asynchronous *PX_READY* signal.

Generation of reset signal for PIOX/PIOX-16 DCM site

TORNADO-P6x provide individual reset signal for PIOX/PIOX-16 interface site, which is controlled by $\overline{PX\_RESET}$ bit of *DSP_PXSX_RESET_RG* IOX register (refer to table 2-11 and section "TMS320C6x DSP Environment" for more details). This allows correct initialization of installed PIOX/PIOX-16 DCM hardware and correct synchronization with host *TORNADO-P6x* DSP software.

Timer/IO pins

PX_TM/XIO-0 and *PX_TM/XIO-1* timer/ IO pins of *TORNADO-P6x* on-board PIOX/PIOX-16 DCM site are connected to *TOUT0/TINP0* and *TOUT1/TINP1* pins of on-board TMS320C6x DSP and can be configured as

either input-only or output-only via on-board J5/J6 jumpers for *TORNADO-P62/P67* DSP systems, via on-board SW4-3/4 switches for *TORNADO-P6202/P6203* DSP systems, and via on-board SW5-1/2 switches for *TORNADO-P64xx* DSP systems.

Refer to figures 2-4a, 2-4b and 2-4c and section "TMS320C6x DSP Environment" earlier in this chapter for more details.

Physical Dimensions for PIOX/PIOX-16 DCM

Physical dimensions for PIOX and PIOX-16 DCM are presented at fig.2-12. This information is intended for those *TORNADO* customers, who need to design custom PIOX/PIOX-16 DCM.

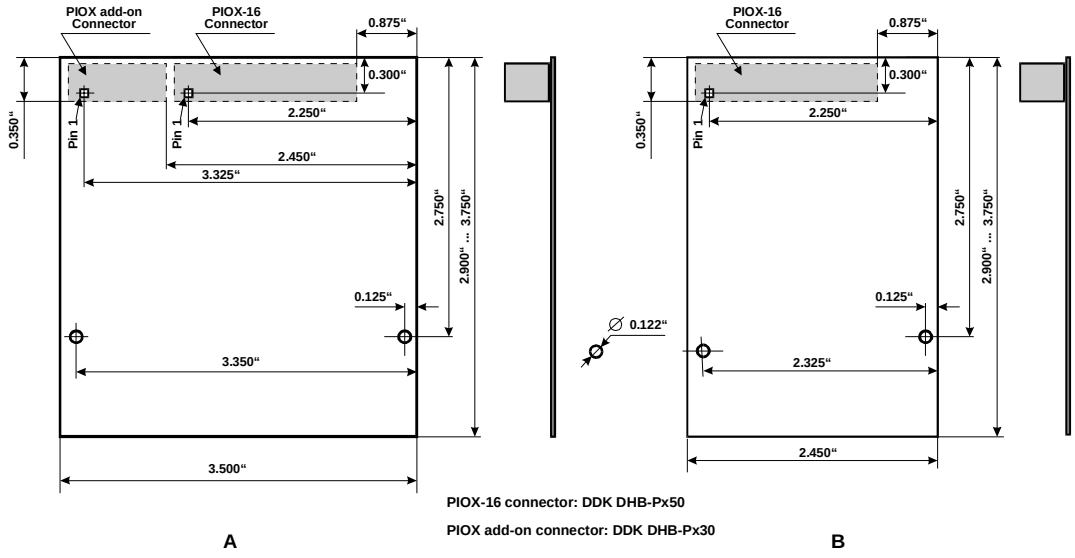


Fig.2-12. Physical dimensions for PIOX (A) and PIOX-16 (B) DCM.

2.5 Serial I/O Expansion DCM Sites (SIOX)

TORNADO-P6x system architecture allows to expand on-board I/O resources and DSP on-chip I/O resources via on-board serial I/O expansion DCM sites (SIOX) (fig.2-2), which are designed for installation of compatible DCM. *TORNADO-P6x* DSP systems provide three on-board SIOX DCM sites, which are compatible with SIOX DCM sites for all *TORNADO* PC plug-in DSP systems and *TORNADO-E/SX/PX* stand-alone DSP controllers and DSP coprocessors.

A variety of 'off-the-shelf' SIOX DCM comprises of AD/DA/DIO and application specific I/O Coprocessors DCM for telecommunication, speech and audio signal processing, industrial and instrumentation, and many more applications.

Connection diagrams and configurations for SIOX DCM sites

TORNADO-P6x DSP systems provides two different types of on-board SIOX DCM sites (refer to fig. 2-2):

- SIOX-A rev.B DCM site (JP4), which comprises of signals for two serial ports (SIO-0 and SIO-1), two timer/IO pins (*SX_TM/XIO-0* and *SX_TM/XIO-1*), external interrupts request inputs (*XIRQ-0, XIRQ-1,* and *XIRQ-2* for *TORNADO-P62xx/P67* DSP systems and *SX_IRQ-0, SX_IRQ-1* and *SX_IRQ-2* for *TORNADO-P64xx* DSP systems), dedicated SIOX-A rev.B/C reset signal, and power supply lines
- Two enhanced SIOX-A rev.C (JP2) and SIOX-B rev.C (JP3) DCM sites, each comprising of the signals for two SIO-0 and SIO-1 serial ports, two timer/IO pins (*SX_TM/XIO-0* and *SX_TM/XIO-1*), external *XIRQ-0* and *XIRQ-1* interrupts request inputs correspondingly for *TORNADO-P62xx/P67* DSP systems and external *SX_IRQ-0* and *SX_IRQ-1* interrupts request inputs correspondingly for *TORNADO-P64xx* DSP systems, dedicated SIOX-A and SIOX-B reset signals correspondingly, 8-bit parallel data bus, 6-bit address bus, parallel data bus control signals, and power supply lines.

Connection diagrams for on-board SIOX DCM sites for different *TORNADO-P6x* DSP systems is presented at figures 2-13a, 2-13b 2-13c and 2-13d.

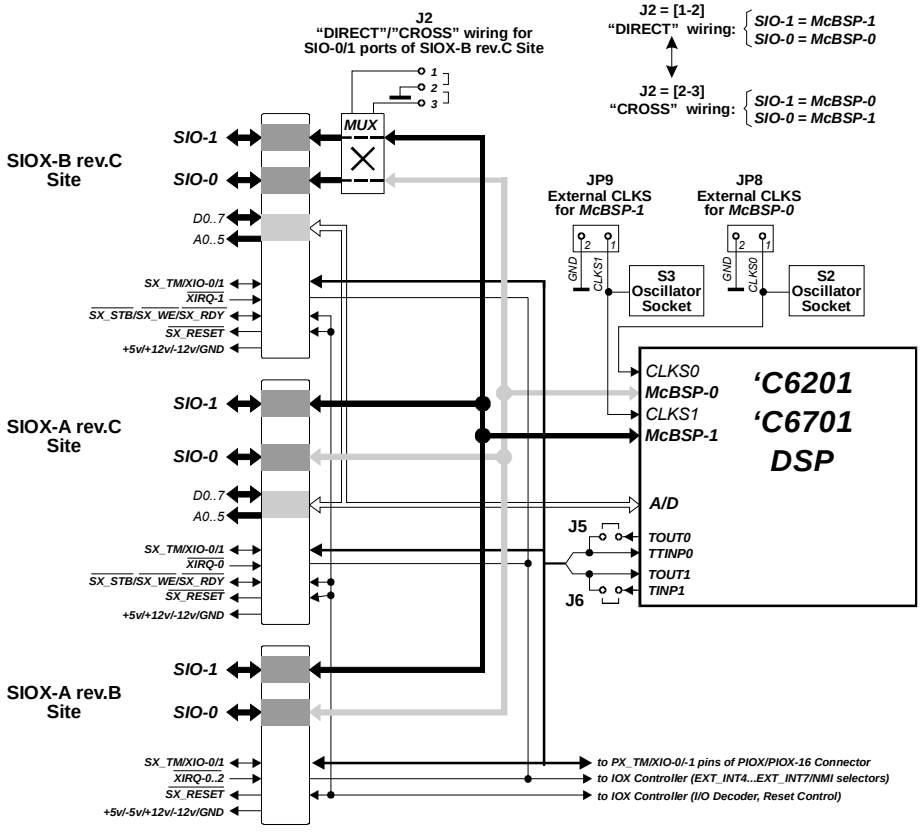


Fig.2-13a. SIOX DCM sites connection diagram for *TORNADO-P62/P67* DSP systems.

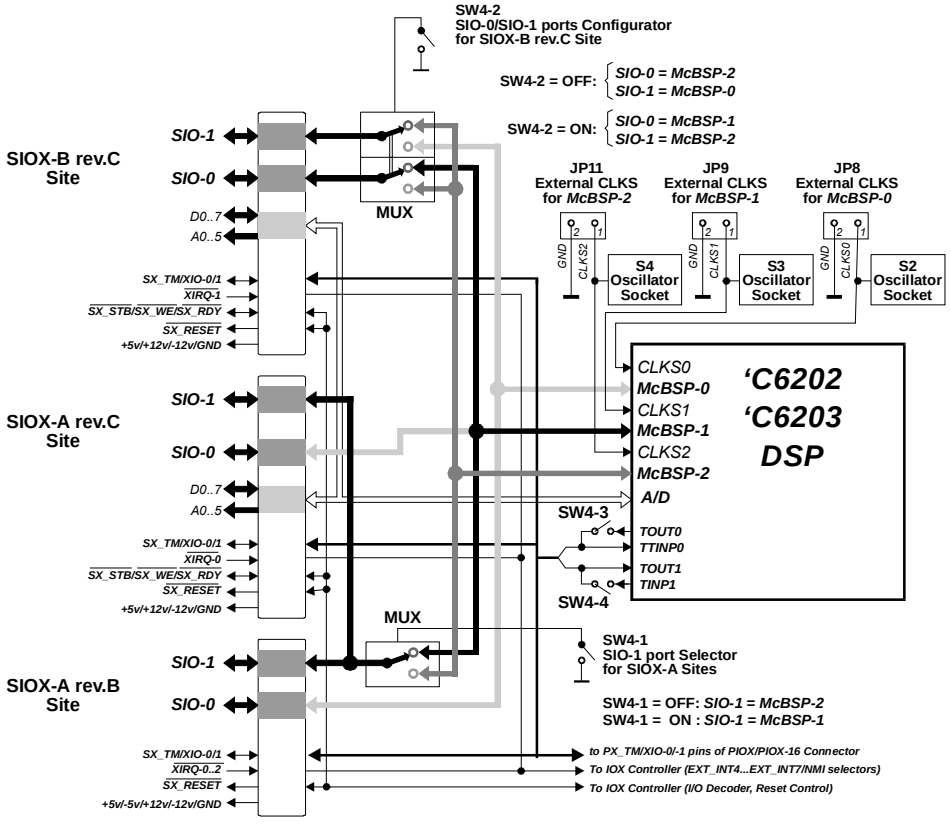


Fig.2-13b. SIOX DCM sites connection diagram for *TORNADO-P6202/P6203* DSP systems.

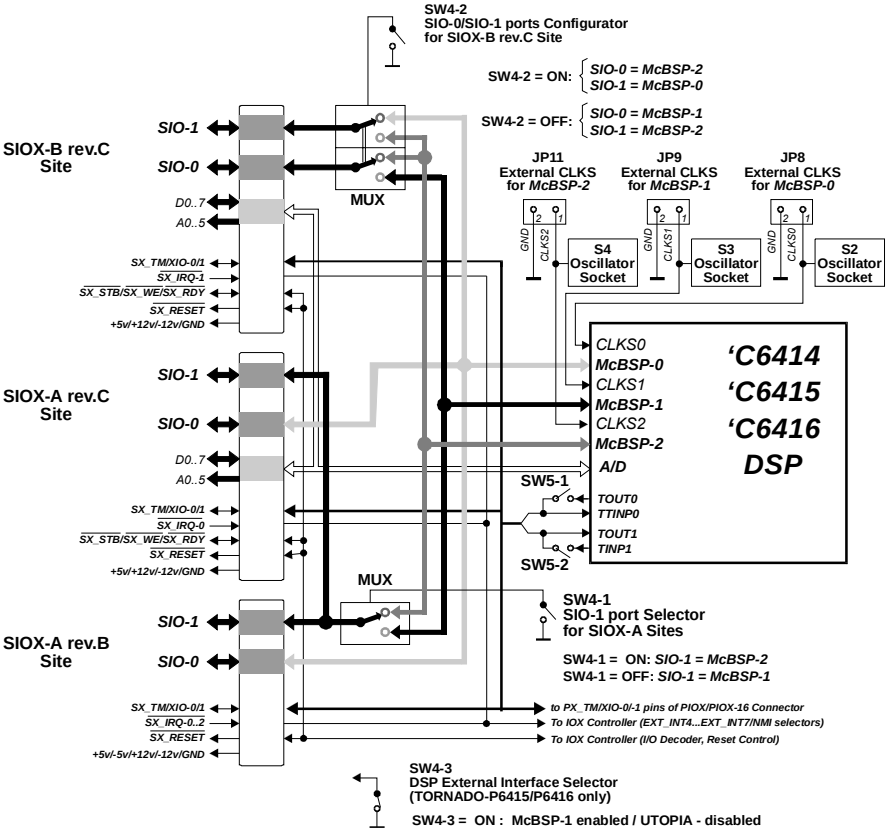


Fig.2-13c. SIOX DCM sites connection diagram for *TORNADO-P6414* DSP systems and *TORNADO-P6415/P6416* DSP systems with disabled DSP on-chip UTOPIA interface.

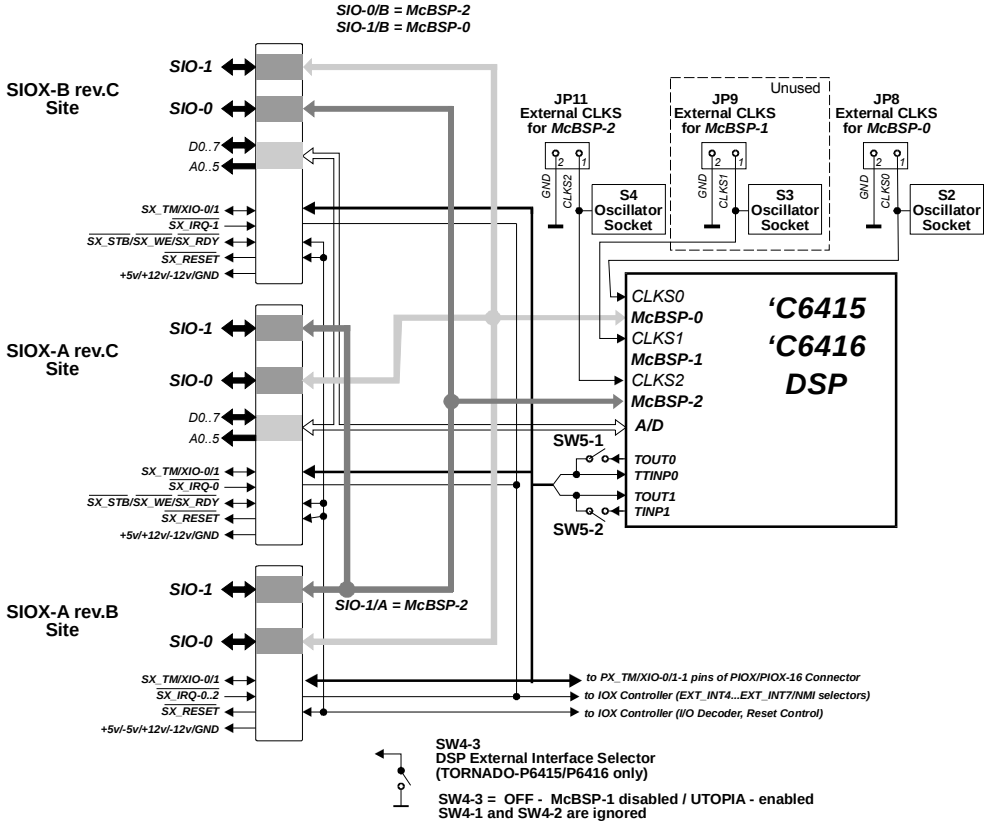


Fig.2-13d. SIOX DCM sites connection diagram for *TORNADO-P6415/P6416* DSP systems with enabled DSP on-chip UTOPIA interface.

For *TORNADO-P62/P67* DSP systems with TMS320C6201/C6701 DSP, which provide two DSP on-chip serial ports (McBSP-0 and McBSP-1), SIO-0 and SIO-1 serial ports of SIOX-A rev.B and SIOX-A rev.C DCM sites are always connected to TMS320C6201/C6701 DSP on-chip McBSP-0 and McBSP-1 serial ports correspondingly. However, SIO-0 and SIO-1 ports of SIOX-B rev.C DCM site of *TORNADO-P62/P67* DSP systems can be configured via on-board J2 jumper to connect to TMS320C6201/C6701 DSP on-chip either McBSP-0 or McBSP-1 serial ports in accordance with table 2-26. Figure 2-14a illustrates different SIO-0/1 serial ports configurations for SIOX-B rev.C DCM sites of *TORNADO-P62/P67* DSP systems.

Table 2-26. SIO-0/1 serial ports configuration for SIOX-B rev.C DCM site of *TORNADO-P62/P67* DSP systems.

J2 jumper setting	SIO-0 port of SIOX-B rev.C DCM site	SIO-1 port of SIOX-B rev.C DCM site	Description
1-2	*McBSP-0*	*McBSP-1*	"DIRECT" wiring for SIO-0/1 serial ports of SIOX-B rev.C DCM site.
2-3	*McBSP-1*	*McBSP-0*	"CROSS" wiring for SIO-0/1 serial ports of SIOX-B rev.C DCM site.

Note: 1. Highlighted configuration corresponds to default factory setting.

For *TORNADO-P6202/P6203* DSP systems with TMS320C6202/C6203 DSP, which provide three DSP on-chip serial ports (McBSP-0, McBSP-1 and McBSP-2), SIO-0 port of SIOX-A rev.B and SIOX-A rev.C DCM sites is always connected to TMS320C6202/C6703 DSP on-chip McBSP-0 serial port.

SIO-1 serial port of SIOX-A rev.B and SIOX-A rev.C DCM sites of *TORNADO-P6202/P6203* DSP systems can be configured via on-board SW4-1 switch to connect to TMS320C6202/C6203 DSP on-chip either McBSP-2 or McBSP-1 serial port in accordance table 2-27. Figure 2-14b illustrates different SIO-1 serial port configurations for SIOX-A rev.B/C DCM sites of *TORNADO-P6202/P6203* DSP systems.

Table 2-27. SIO-1 serial port configuration for SIOX-A rev.B/C DCM site of *TORNADO-P6202/P6203* DSP systems.

SW4-1 switch setting	SIO-1 port of SIOX-A rev.B/C DCM site
OFF	*McBSP-2*
ON	*McBSP-1*

Note: 1. Highlighted configuration corresponds to default factory setting.

SIO-0 and SIO-1 serial ports of SIOX-B rev.C DCM site of *TORNADO-P6202/P6203* DSP systems can be configured via on-board SW4-2 switch to connect to either DSP on-chip McBSP-2 and McBSP-0 serial ports correspondingly, or to DSP on-chip McBSP-1 and McBSP-2 serial ports correspondingly in accordance with table 2-28. Other configurations for SIO-0 and SIO-1 serial ports of SIOX-B rev.C DCM site of *TORNADO-P6202/P6203* DSP systems are not available. Figure 2-14c illustrates different SIO-0/1 serials port configurations for SIOX-B rev.C DCM site of *TORNADO-P6202/P6203* DSP systems.

Table 2-28. SIO-0/1 serial ports configuration for SIOX-B rev.C DCM site of *TORNADO-P6202/P6203* DSP systems.

SW4-2 switch setting	SIO-0 port of SIOX-B rev.C DCM site	SIO-1 port of SIOX-B rev.C DCM site
OFF	*McBSP-2*	*McBSP-0*
ON	*McBSP-1*	*McBSP-2*

Note: 1. Highlighted configuration corresponds to default factory setting.

For *TORNADO-P6415/P6416* DSP systems with on-board TMS320C6415/C6416 DSP, which provide three DSP on-chip serial ports (McBSP-0, McBSP-1 and McBSP-2) with the McBSP-1 serial port being alternatively selected with DSP on-chip UTOPIA interface via on-board SW4-3 switch (refer to table 2-14 and section "TMS320C6x DSP Environment" earlier in this chapter), several options are available as described below upon the enable status of DSP on-chip UTOPIA interface.

For *TORNADO-P6414* DSP systems with on-board TMS320C6414 DSP, which provide three DSP on-chip serial ports (McBSP-0, McBSP-1 and McBSP-2) without DSP on-chip UTOPIA interface, available configurations of serial ports for on-board SIOX-A/B DCM sites correspond to that for *TORNADO-P6415/P6416* DSP systems with disabled DSP on-chip UTOPIA interface.

For all *TORNADO-P64xx* DSP systems, SIO-0 port of SIOX-A rev.B and SIOX-A rev.C DCM sites is always connected to TMS320C64xx DSP on-chip McBSP-0 serial port.

For *TORNADO-P6414* DSP systems and *TORNADO-P6415/P6416* DSP systems with disabled DSP on-chip UTOPIA interface, SIO-1 serial port of SIOX-A rev.B and SIOX-A rev.C DCM sites can be configured via on-board SW4-1 switch to connect to TMS320C64xx DSP on-chip either McBSP-2 or McBSP-1 serial port in accordance table 2-29. These options are similar to that for *TORNADO-P6202/P6203* DSP systems. Figure 2-14d illustrates different SIO-1 serial port configurations for SIOX-A rev.B/C DCM sites of *TORNADO-P6414* DSP systems and of *TORNADO-P6415/P6416* DSP systems with disabled DSP on-chip UTOPIA interface.

However, in case TMS320C6415/C6416 DSP on-chip UTOPIA interface is enabled for *TORNADO-P6415/P6416* DSP systems, then SIO-1 serial port of SIOX-A rev.B and SIOX-A rev.C DCM sites always connects to DSP on-chip McBSP-2 serial port and on-board SW4-1 switch setting is ignored. Figure 2-14f illustrates SIO-1 serial port configuration for SIOX-A rev.B/C DCM sites of *TORNADO-P6415/P6416* DSP systems with enabled DSP on-chip UTOPIA interface.

Table 2-29. SIO-1 serial port configuration for SIOX-A rev.B/C DCM site of *TORNADO-P64xx* DSP systems.

SW4-1 switch setting	**SIO-1 port of SIOX-A rev.B/C DCM site for *TORNADO-P6414* DSP systems and for *TORNADO-P6415/P6416* DSP systems with disabled DSP on-chip UTOPIA interface**	**SIO-1 port of SIOX-A rev.B/C DCM site for *TORNADO-P6415/P6416* DSP systems with enabled DSP on-chip UTOPIA interface**
ON	*McBSP-2*	*McBSP-2*
OFF	*McBSP-1*	*McBSP-2*

Note: 1. Highlighted configuration corresponds to default factory setting.

For *TORNADO-P6414* DSP systems and *TORNADO-P6415/P6416* DSP systems with disabled DSP on-chip UTOPIA interface, SIO-0 and SIO-1 serial ports of SIOX-B rev.C DCM site can be configured via on-board SW4-2 switch to connect to either DSP on-chip McBSP-2 and McBSP-0 serial ports correspondingly, or to DSP on-chip McBSP-1 and McBSP-2 serial ports correspondingly in accordance with table 2-30. Other configurations for SIO-0 and SIO-1 serial ports of SIOX-B rev.C DCM site are not available for *TORNADO-P6414* DSP systems and *TORNADO-P6415/P6416* DSP systems with disabled DSP on-chip UTOPIA interface. Figure 2-14e illustrates different SIO-0/1 serials port configurations for SIOX-B rev.C DCM site for *TORNADO-P6414* DSP systems and for *TORNADO-P6415/P6416* DSP systems with disabled DSP on-chip UTOPIA interface.

However, in case TMS320C6415/C6416 DSP on-chip UTOPIA interface is enabled for *TORNADO-P6415/P6416* DSP systems, then SIO-0 and SIO-1 serial ports of SIOX-B rev.C DCM site always connect to DSP on-chip McBSP-2 and McBSP-0 serial ports correspondingly, and on-board SW4-2 switch setting is ignored. Figure 2-14f illustrates SIO-0/1 serial ports configuration for SIOX-B rev.C DCM site of *TORNADO-P6415/P6416* DSP systems with enabled DSP on-chip UTOPIA interface.

Table 2-30. SIO-0/1 serial ports configuration for SIOX-B rev.C DCM site of *TORNADO-P64xx* DSP systems.

SW4-2 switch setting	**SIO-0/1 ports of SIOX-B rev.C DCM site for *TORNADO-P6414* DSP systems and for *TORNADO-P6415/P6416* DSP systems with disabled DSP on-chip UTOPIA interface**		**SIO-0/1 ports of SIOX-B rev.C DCM site for *TORNADO-P6415/P6416* DSP systems with enabled DSP on-chip UTOPIA interface**	
	SIO-0 port	**SIO-1 port**	**SIO-0 port**	**SIO-1 port**
ON	*McBSP-2*	*McBSP-0*	*McBSP-2*	*McBSP-0*
OFF	*McBSP-1*	*McBSP-2*	*McBSP-2*	*McBSP-0*

Note: 1. Highlighted configuration corresponds to default factory setting.

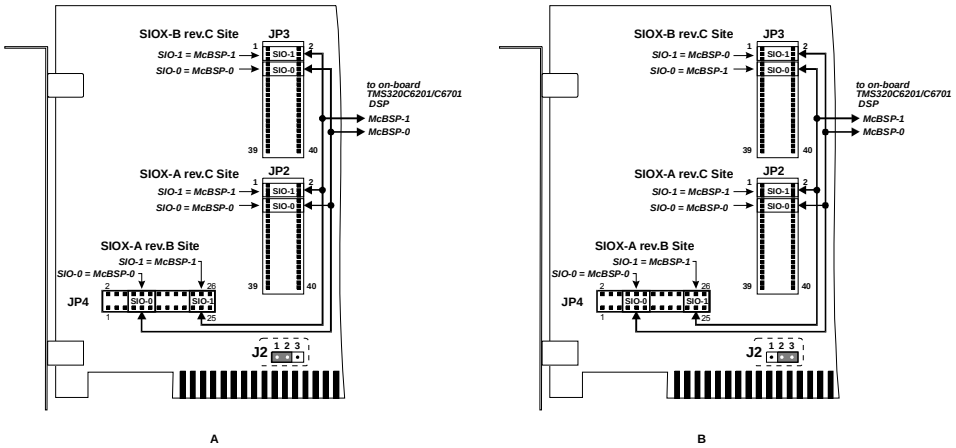


Fig. 2-14a. "Direct" (A) and "Cross" (B) wiring configurations of SIO-0/1 serial ports for SIOX-B rev.C DCM site of *TORNADO-P62/P67* DSP systems.

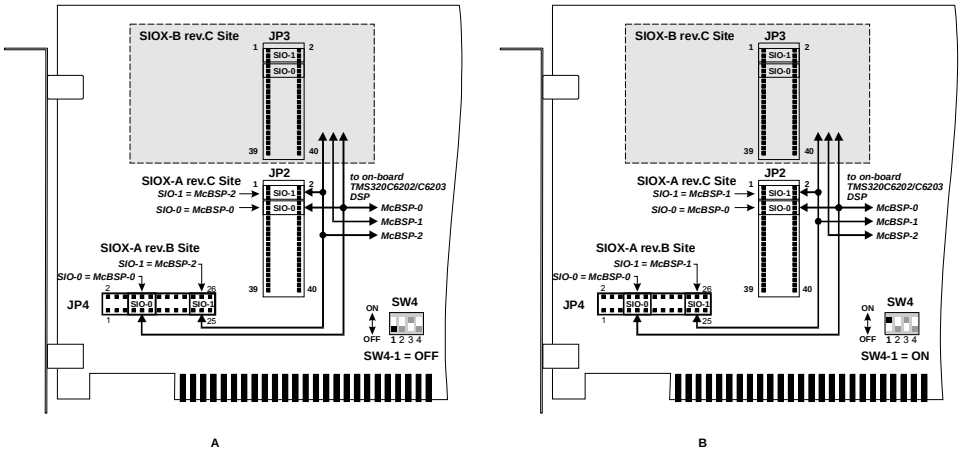


Fig. 2-14b. SIO-1 serial port configurations for SIOX-A rev.B/C DCM sites of *TORNADO-P6202/P6203* DSP systems.

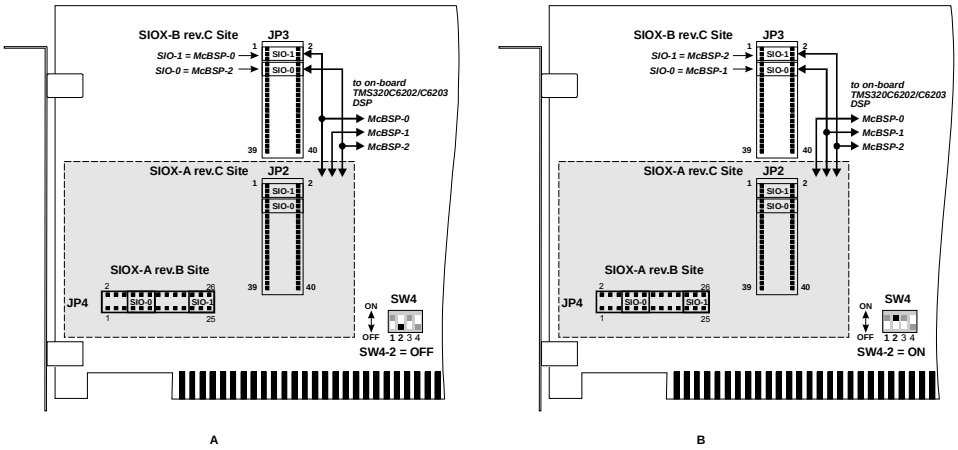


Fig. 2-14c. SIO-0/1 serial port configurations for SIOX-B rev.C DCM site of *TORNADO-P6202/P6203* DSP systems.

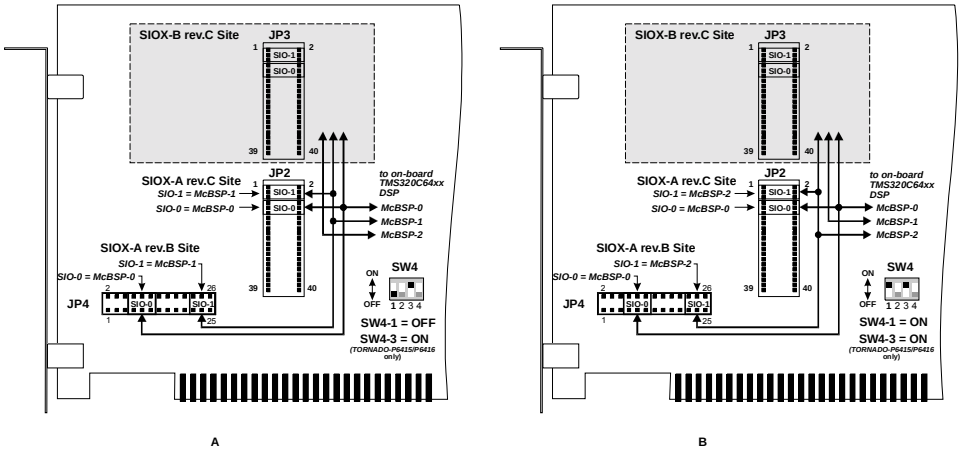


Fig. 2-14d. SIO-1 port configurations for SIOX-A rev.B/C DCM sites of *TORNADO-P6414* DSP systems and of *TORNADO-P6415/P6416* DSP systems with disabled DSP on-chip UTOPIA interface.

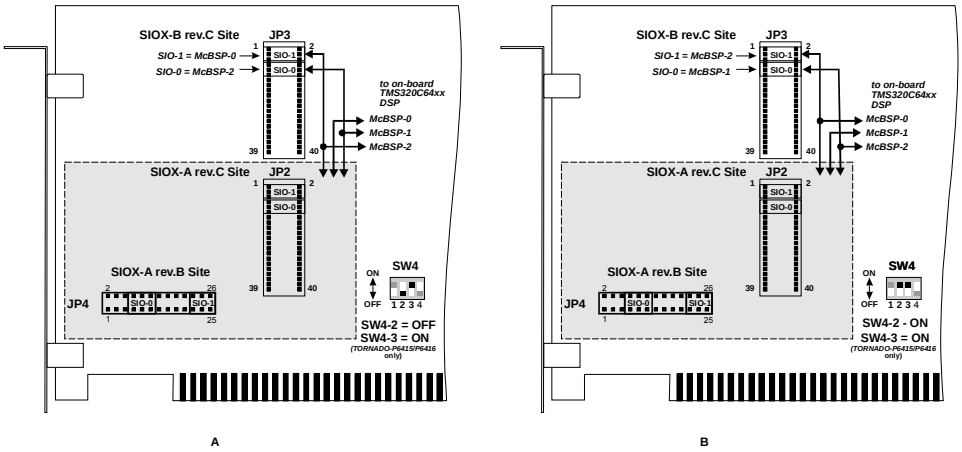


Fig. 2-14e. SIO-0/1 serial ports configurations for SIOX-B rev.C DCM site of *TORNADO-P6414* DSP systems and of *TORNADO-P6415/P6416* DSP systems with disabled DSP on-chip UTOPIA interface.

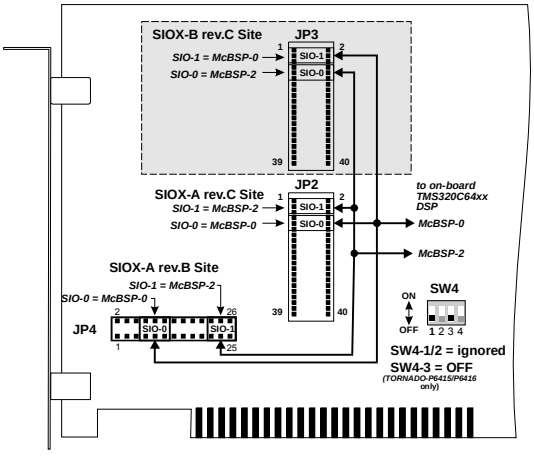


Fig. 2-14f. SIO-0/1 serial ports configuration for SIOX-B rev.C DCM site of *TORNADO-P6415/P6416* DSP systems with enabled DSP on-chip UTOPIA interface.

Maximum serial data transfer speed for SIOX DCM sites

Maximum serial data transfer speed via SIO-0 and SIO-1 serial ports of SIOX DCM sites for *TORNADO-P6x* DSP systems is as the following:

- 200 Mbit/s for *TORNADO-P62* DSP systems
- 167 Mbit/s for *TORNADO-P67* DSP systems
- 250 Mbit/s for *TORNADO-P6202* DSP systems
- 300 Mbit/s for *TORNADO-P6203* DSP systems
- 600 Mbit/s for *TORNADO-P64xx* DSP systems.

Installation of SIOX DCM onto TORNADO-P6x mainboard

Figure 2-15 shows installation examples of different SIOX DCM onto *TORNADO-P6x* mainboards. External analog and digital I/O signals for installed SIOX DCM have to be connected by means of on-board SIOX DCM I/O connector via rear mounting bracket of *TORNADO-P6x* DSP system.

CAUTION

TORNADO-P6x on-board area for SIOX-A rev.B DCM is shared with the on-board area for SIOX-A rev.C and SIOX-B rev.C DCM. Either SIOX-A rev.B DCM or SIOX-A rev.C and SIOX-B rev.C DCM can be installed onto *TORNADO-P6x* mainboard.

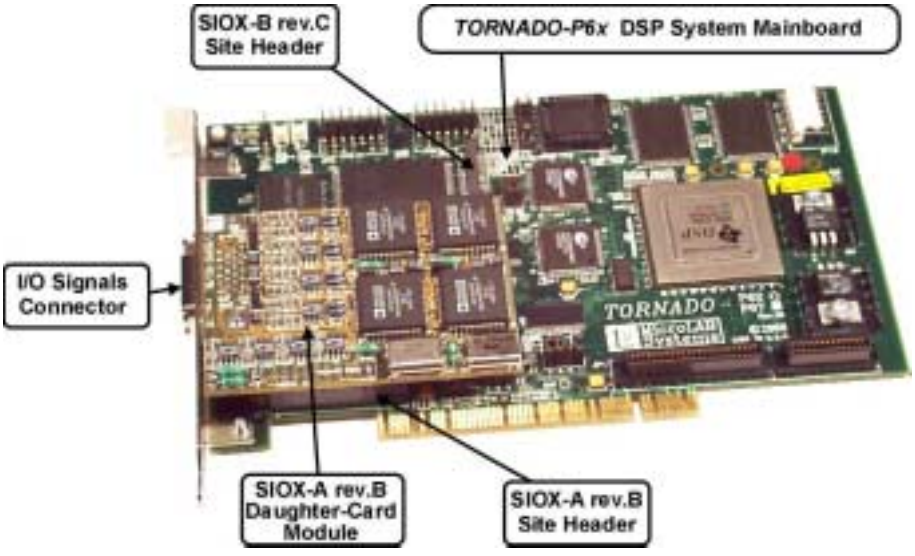


Fig.2-15a. TORNADO-P6x mainboard with SIOX-A rev.B DCM.

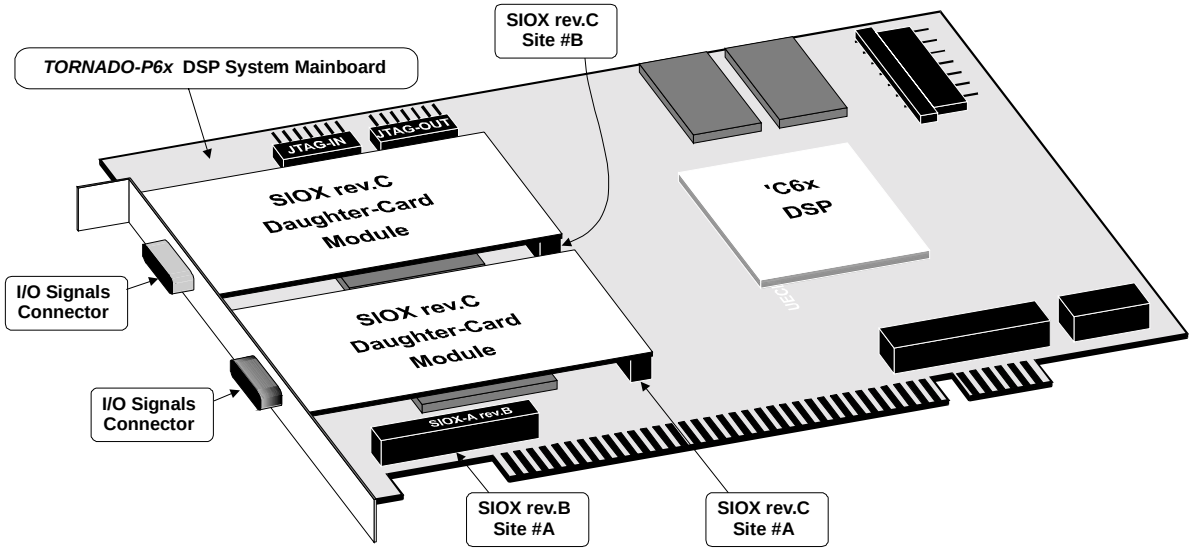


Fig.2-15b. TORNADO-P6x mainboard with SIOX-A rev.C and SIOX-B rev.C DCM.

SIOX-A rev.B DCM site interface connector

TORNADO-P6x on-board SIOX-A rev.B DCM site connector (JP4) is an industry standard dual-row 26-pin female header with 0.1"x0.1" pin pattern. SIOX-A rev.B DCM site interface connector pinout is presented at fig.2-16 and signal specifications are listed in table 2-31.

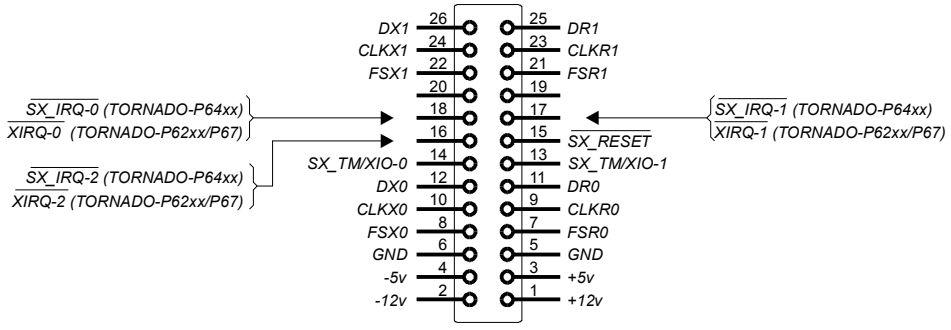


Fig.2-16. SIOX-A rev.B DCM site interface connector pinout (top view).

Table 2-31. SIOX-A rev.B DCM site interface connector signal specification.

signal name	signal type	description
		SIO-0 port control
DX0 *FSX0* *CLKX0*	O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port of SIOX rev.B DCM site.
DR0 *FSR0* *CLKR0*	I I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-0 port of SIOX rev.B DCM site.
		SIO-1 port control
DX1 *FSX1* *CLKX1*	O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port of SIOX rev.B DCM site.
DR1 *FSR1* *CLKR1*	I I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-1 port of SIOX rev.B DCM site.
		DSP Timers, Reset and Interrupt Requests
SX_TM/XIO-0 *SX_TM/XIO-1*	I/O/Z	Timer or I/O pins, which are connected to the corresponding TMS320C6x DSP on-chip timer I/O pins (TOUT0/TINP0 and TOUT1/TINP1). Each of these pins can be used as timer input, timer output, or general purpose I/O pin. Refer to figures 2-4a, 2-4b and 2-4c and section “TMS320C6x DSP Environment” earlier in this chapter for more details.
$\overline{SX\_RESET}$	O	Active low reset signal for SIOX-A rev.B/C DCM sites, which is controlled via $\overline{SXA\_RESET}$ bit of *DSP_PXSX_RESET_RG* IOX register (refer to table 2-11 and section “TMS320C6x DSP Environment” earlier in this chapter for more details).

$\overline{XIRQ-0}$ $\overline{XIRQ-1}$ $\overline{XIRQ-2}$ *(TORNADO-P62x/P67)* *or* $\overline{SX\_IRQ-0}$, $\overline{SX\_IRQ-1}$ $\overline{SX\_IRQ-2}$ *(TORNADO-P64xx)*	I	Active low pulled-up interrupt request inputs from SIOX-A rev.B DCM site, which can be routed to external interrupt request inputs for on-board TMS320C6x DSP using DSP external interrupt selector registers(*DSP_EXT_INT4_SEL_RG*.. *DSP_EXT_INT7_SEL_RG* and *DSP_NMI_SEL_RG* IOX registers). Refer to table 2-12 and section "TMS320C6x DSP Environment" for more details. *TORNADO-P62xx/P67* DSP systems provide three SIOX interrupt request inputs ($\overline{XIRQ-0}$, $\overline{XIRQ-1}$, and $\overline{XIRQ-2}$) with the $\overline{XIRQ-2}$ interrupt request input, which are shared with the corresponding interrupt request input of on-board PIOX/PIOX-16 DCM site. *TORNADO-P64xx* DSP systems provide three dedicated SIOX interrupt request inputs ($\overline{SX\_IRQ-0}$, $\overline{SX\_IRQ-1}$, and $\overline{SX\_IRQ-2}$), which are not shared with interrupt request inputs from on-board PIOX/PIOX-16 DCM site.
Power Supplies		
GND		Ground.
+5v		+5v power (from PCI-bus or external power connector JP10).
+12v		+12v power (from PCI-bus or external power connector JP10).
-5v		-5v power (from on-board voltage regulator sourced from –12v on-board power).
-12v		-12v power (from PCI-bus or external power connector JP10).

Note:
1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
2. All logic I/O signal levels and load currents correspond to that for 3v/5v TTL logic.

SIOX-A/B rev.C DCM sites interface connector

TORNADO-P6x on-board SIOX-A/B rev.C DCM sites interface connectors (JP2 and JP3) are high-density Samtec dual-row 50-pin female headers with 0.05"x0.05" pin pattern from Samtec Inc (www.samtec.com). Compatible SIOX rev.C plugs (Samtec p/n TFM-120-22-S-D-LC) for design of custom SIOX rev.B DCM are available from MicroLAB Systems upon request.

SIOX rev.C DCM site interface connector pinout is presented at fig.2-17 and signal specifications are provided in table 2-32.

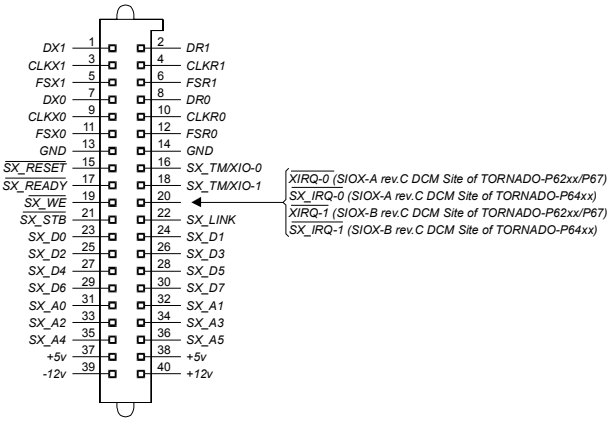


Fig.2-17. SIOX rev.C DCM site interface connector pinout (top view).

Table 2-32. SIOX rev.C DCM site interface connector signal specification.

signal name	signal type	Description
		SIO-0 port control
DX0 *FSX0* *CLKX0*	O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port of SIOX rev.C DCM site.
DR0 *FSR0* *CLKR0*	I I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-0 port of SIOX rev.C DCM site.
		SIO-1 port control
DX1 *FSX1* *CLKX1*	O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port of SIOX rev.C DCM site.
DR1 *FSR1* *CLKR1*	I I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-1 port of SIOX rev.C DCM site.
		DSP Timers, Reset and Interrupt Requests
SX_TM/XIO-0 *SX_TM/XIO-1*	I/O/Z	Timer or I/O pins, which are connected to the corresponding TMS320C6x DSP on-chip timer I/O pins (TOUT0/TINP0 and TOUT1/TINP1). Each of these pins can be used as timer input, timer output, or general purpose I/O pin. Refer to figures 2-4a, 2-4b and 2-4c and section “TMS320C6x DSP Environment” earlier in this chapter for more details.

$\overline{SX\_RESET}$	O	Active low reset signal for SIOX-A and SIOX-B rev.C DCM sites, which is controlled via $\overline{SXA\_RESET}$ and $\overline{SXB\_RESET}$ bits correspondingly bit of *DSP_PXSX_RESET_RG* IOX register (refer to table 2-11 and section "TMS320C6x DSP Environment" earlier in this chapter for more details).
$\overline{XIRQ-0}$ *(SIOX-A rev.C DCM site of TORNADO-P62xx/P67)* $\overline{SX\_IRQ-0}$ *(SIOX-A rev.C DCM site of TORNADO-P64xx)* $\overline{XIRQ-1}$ *(SIOX-B rev.C DCM site of TORNADO-P62xx/P67)* $\overline{SX\_IRQ-1}$ *(SIOX-B rev.C DCM site of TORNADO-P64xx)*	I	Active low pulled-up interrupt request inputs from SIOX-A and SIOX-B rev.C DCM sites, which can be routed to external interrupt request inputs for on-board TMS320C6x DSP using DSP external interrupt selector registers(*DSP_EXT_INT4_SEL_RG.. DSP_EXT_INT7_SEL_RG* and *DSP_NMI_SEL_RG* IOX registers). Refer to table 2-12 and section "TMS320C6x DSP Environment" for more details. *TORNADO-P62xx/P67* DSP systems provide $\overline{XIRQ-0}$ and $\overline{XIRQ-1}$ interrupt request inputs from SIOX-A and SIOX-B rev.C DCM sites correspondingly, which are shared with the corresponding interrupt request inputs of on-board PIOX/PIOX-16 DCM site. $\overline{XIRQ-0}$ and $\overline{XIRQ-1}$ interrupt request inputs are also shared with interrupt request inputs from SIOX-A rev.B DCM site. *TORNADO-P64xx* DSP systems provide dedicated $\overline{SX\_IRQ-0}$, and $\overline{SX\_IRQ-1}$ interrupt request inputs from SIOX-A and SIOX-B rev.C DCM sites correspondingly, which are not shared with interrupt request inputs from on-board PIOX/PIOX-16 DCM site. $\overline{SX\_IRQ-0}$, and $\overline{SX\_IRQ-1}$ interrupt request inputs are shared with interrupt request inputs from SIOX-A rev.B DCM site.
SX_LINK	I/O	This optional pin can be used for communication or synchronization between two DCM, which are installed into SIOX-A rev.C DCM site and SIOX-B rev.C DCM site. *SX_LINK* pins of SIOX-A rev.C site and SIOX-B rev.C site are directly connected without any buffers and pull-up/down resistors.
8-bit Parallel Data Bus		
SX_D[0..7]	I/O	SIOX rev.C DCM site interface data bus.
SX_A[0..5]	O	SIOX rev.C DCM site interface address bus.
$\overline{SX\_STB}$	O	Active low data transfer strobe for parallel data bus of SIOX rev.C DCM site interface. Each of SIOX-A rev.C DCM site and SIOX-B rev.C DCM site has its own data transfer strobe, which is generated when *TORNADO-P6x* on-board DSP performs access either to SIOX-A or SIOX-B rev.C DCM site area of DSP memory map in accordance with table 2-1.
$\overline{SX\_WE}$	O	Active low SIOX rev.C DCM site interface write enable signal.
$\overline{SX\_READY}$	I	Active low pulled-up common data ready acknowledge signal for both SIOX-A rev.C DCM site and SIOX-B rev.C DCM site, which must be generated by addressed SIOX rev.C DCM in order to terminate current SIOX rev.C parallel data bus access cycle in accordance with the timing requirements for SIOX rev.C DCM site parallel interface. Each of installed SIOX rev.C DCM shall keep this output signal in the Z-state until particular SIOX rev.C DCM is not selected via the corresponding data transfer strobe.

Power Supplies		
GND		Ground.
+5v		+5v power (from PCI-bus or external power connector JP10).
+12v		+12v power (from PCI-bus or external power connector JP10).
-12v		-12v power (from PCI-bus or external power connector JP10).

Note:
1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
2. All logic I/O signal levels and load currents correspond to that for 3v/5v TTL logic.

Generation of reset signal for SIOX DCM sites

TORNADO-P6x DSP systems provide individual reset signals for SIOX-A rev.B/C and SIOX-B rev.C DCM site interfaces, which are controlled by $\overline{SXA\_RESET}$ and $\overline{SXB\_RESET}$ bits of *DSP_PXSX_RESET_RG* IOX register (refer to table 2-1 and section "TMS320C6x DSP Environment" earlier in this chapter for more details). This allows correct initialization of installed SIOX rev.B/C DCM hardware and correct synchronization with *TORNADO-P6x* DSP software.

Connection of external serial clock to TMS320C6x DSP McBSP serial ports

TORNADO-P6x DSP systems allow connection of individual external clock sources to all TMS320C6x DSP on-chip McBSP serial ports (McBSP-0/1 ports for *TORNADO-P62/P67* DSP systems and McBSP-0/1/2 ports for *TORNADO-P6202/P6203/P64xx* DSP systems). These clocks are known as CLKS-0 and CLKS-1 signals in accordance with TI TMS320C6201/C6701 McBSP serial port specifications, and as CLKS-0, CLKS-1 and CLKS-2 signals in accordance with TI TMS320C6202/C6203/C64xx McBSP serial port specifications.

External CLKS clocks for the DSP on-chip McBSP serial ports delivers outstanding flexibility for generation of virtually any data transfer frequency for DSP on-chip McBSP serial ports in order to meet requirements of any application.

External clock source signals CLKS-0/1/2 for each of the McBSP-0/1/2 serial ports can be connected independently and are available from the following external sources:

- from external source via on-board JP8 (for McBSP-0 port), JP9 (for McBSP-1 port) and JP10 (for McBSP-2 port for *TORNADO-P6202/P6203/P64xx* DSP systems only) connectors (refer to fig.2-2, fig.2-18a and fig.A-1)
- from 5v TTL/CMOS crystal oscillators in 4-pins DIP-8 IC package, which can be installed into on-*TORNADO-P6x* board S2 socket (for McBSP-0 port), S3 socket (for McBSP-1 port) and S4 socket (for McBSP-2 port for *TORNADO-P6202/P6203/P64xx* DSP systems only) (refer to fig.2-2, fig.2-18b, fig.2-18c and fig.A-1).

Location and pinout for on-board JP8/JP9/JP18 connectors and on-board S2/S3/S4 oscillator sockets for connection of external serial port clock source signals (CLKS-0/1/2) for DSP on-chip McBSP-0/1/2 serial ports are shown at figure 2-18.

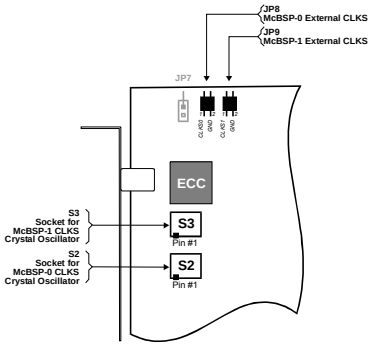


Fig. 2-18a. McBSP-0/McBSP-1 external serial clock connectors and crystal oscillator sites at *TORNADO-P62/P67* mainboard.

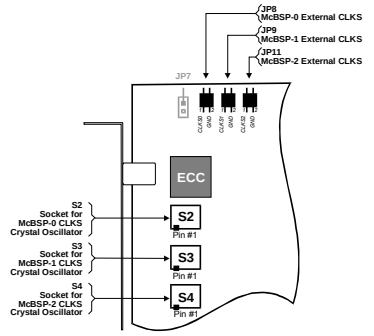


Fig. 2-18b. McBSP-0/McBSP-1/McBSP-2 external serial clock connectors and crystal oscillator sites at *TORNADO-P6202/P6203* mainboard.

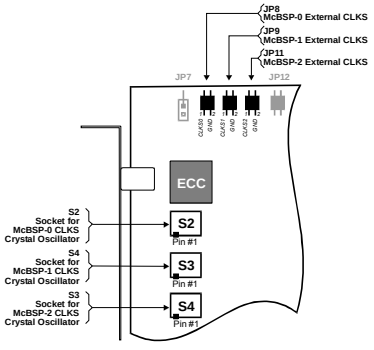


Fig. 2-18c. McBSP-0/McBSP-1/McBSP-2 external serial clock connectors and crystal oscillator sites at *TORNADO-P64xx* mainboard.

Selection of the CLKS-0/1/2 external source clock as the source clock for the McBSP-0/1/2 instead of DSP clock can be done by DSP application via programming the corresponding DSP on-chip McBSP-0/1/2 control registers. Refer to original TI TMS320C6x documentation for getting more information on programming the McBSP serial ports.

Parallel data transfer timing for SIOX rev.C DCM site interface

Timing diagram for parallel data transfer via SIOX rev.C DCM site interface site is presented at fig.2-19. This data transfer timing is known as the industry standard MOTO mode and assumes usage of data strobe signal and write enable signal.

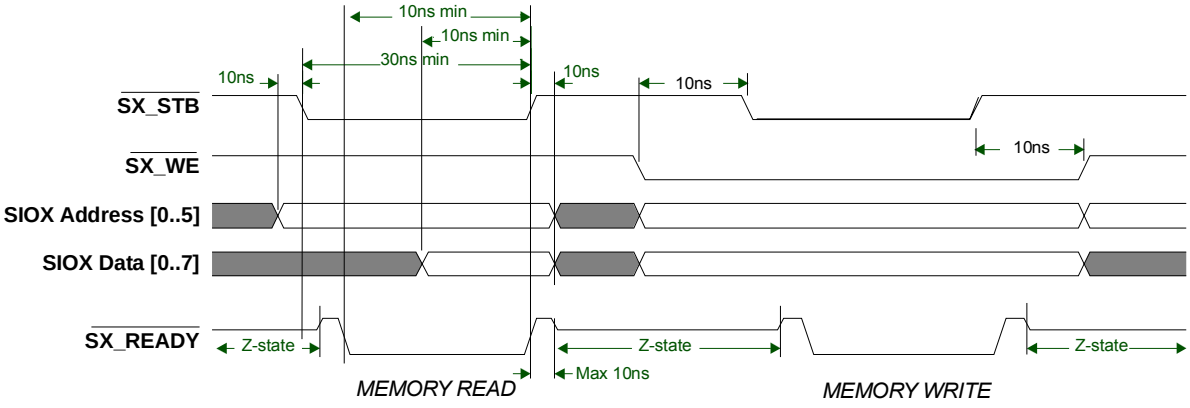


Fig.2-19. Timing diagram for parallel data transfer via SIOX rev.C DCM site interface.

CAUTION

Minimum time duration for parallel data transfer strobe of SIOX rev.C DCM site interface must be 25ns (30ns is recommended) with setup/hold times 10ns. Data transfer acknowledgement is performed by means of asynchronous *SX_READY* signal.

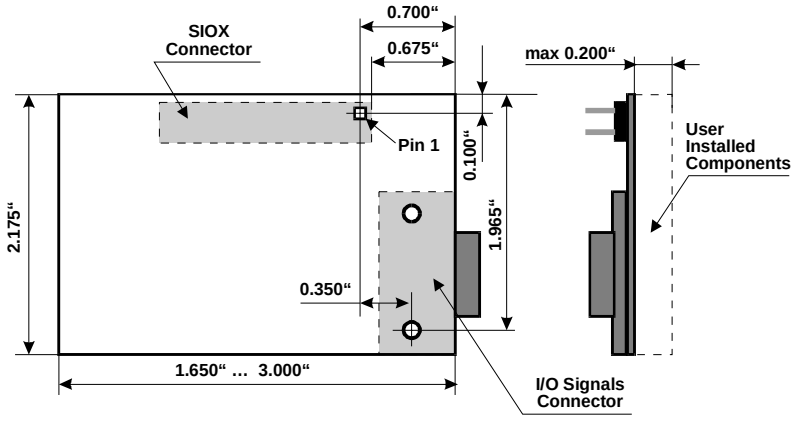
Timer/IO pins

SX_TM/XIO-0 and *SX_TM/XIO-1* timer/ IO pins of *TORNADO-P6x* on-board SIOX rev.B/C DCM sites are connected to *TOUT0/TINP0* and *TOUT1/TINP1* pins of on-board TMS320C6x DSP and can be configured as either input-only or output-only via on-board J5/J6 jumpers for *TORNADO-P62/P67* DSP systems, via on-board SW4-3/4 switches for *TORNADO-P6202/P6203* DSP systems, and via on-board SW5-1/2 switches for *TORNADO-P64xx* DSP systems.

Refer to figures 2-4a, 2-4b and 2-4c and section “TMS320C6x DSP Environment” earlier in this chapter for more details.

Physical Dimensions for SIOX DCM

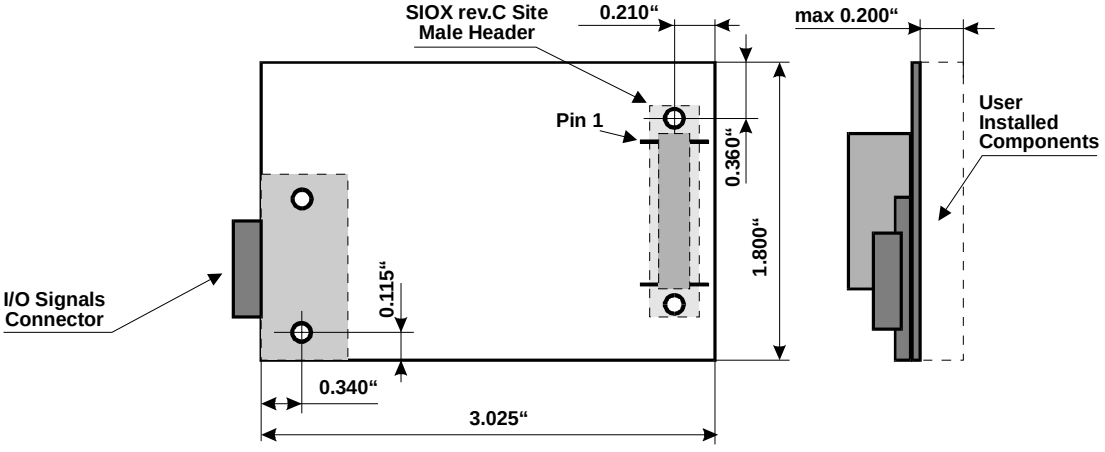
Physical dimensions for SIOX rev.B and SIOX rev.C DCM are presented at fig.2-20. This information is intended for those *TORNADO* customers, who need to design custom SIOX DCM.



SIOX connector: 20-pin or 26-pin straight dual-row mail header (0.025“ Sq., 0.1“x0.1” pattern)

Recommended connector for Analog I/O: DDK DHA-RC14-R122N
DDK DHA-RC20-R122N
DDK DHA-RC26-R122N

Fig.2-20a. Physical dimensions for SIOX rev.B DCM.



SIOX rev.C Site Male Header: SAMTEC TFM-120-22-S-D-LC

Recommended connector for Analog I/O: DDK DHA-RC26-R122N

Fig.2-20b. Physical dimensions for SIOX rev.C DCM.

2.6 Emulation Tools for *TORNADO-P6x*

TORNADO-P6x DSP systems use scan-path emulation technique for debugging on-board TMS320C6x DSP environment and DSP application software. Compatible scan-path emulation tools, which can be used with *TORNADO-P6x* are as the following:

- TI XDS (XDS510, XDS560, etc) or MicroLAB Systems *MIRAGE* (*MIRAGE-510DX*, *MIRAGE-P510D*, etc), hereafter *external JTAG emulators*, which connect to *TORNADO-P6x* DSP systems via on-board JTAG-IN connector
- *TORNADO-P6x* on-board emulation controller chip (*ECC*, also known as TBC)
- TI C6000 Code Composer Studio IDE as the debugging environments for TMS320 DSP, which run with all emulator tools (*ECC* and external JTAG emulators).

CAUTION

Selection between external JTAG emulator and *TORNADO-P6x* on-board *ECC* emulation controller, which will be used for debugging the on-board DSP environment via DSP on-chip JTAG port, is performed via on-board JTAG port multiplexer, which is controlled by *TP6CC.EXE* PC DOS software utility (or *TCC.EXE TSDK* Windows utility) using *-ex* and *-ei* command line options. Refer to chapter 4 for more details about software utilities for *TORNADO-P6x* DSP systems.

Both external JTAG emulator and *TORNADO-P6x* on-board *ECC* emulation controller deliver identical emulation capabilities when debugging the on-board DSP environment via DSP on-chip JTAG port using TI C6000 Code Composer Studio IDE. However, in case customer application assumes intensive communication between *TORNADO-P6x* DSP systems and host PCI-bus environment, it is recommended to use external JTAG emulator (which must be plugged into the neighbor PC), since this will provide higher host PC Windows system safety and integrity.

TORNADO-P6x on-board JTAG path for connection to external JTAG emulator

TORNADO-P6x on-board JTAG path for connection to external JTAG emulator is presented at figure 2-21 (see also fig. 2-1, fig.2-2 and fig. A-1) and comprises of JTAG-IN connector (JP5), TMS320C6x JTAG port, JTAG-OUT connector (JP6) and JTAG path terminator (J4 jumper for *TORNADO-P62/P67* DSP systems, SW6-1 switch for *TORNADO-P6202/P6203* DSP systems, and SW4-4 switch for *TORNADO-P64xx* DSP systems).

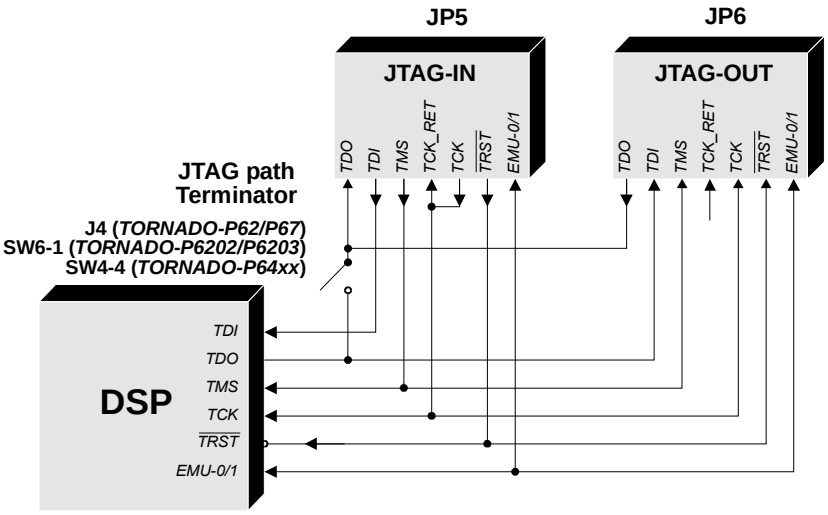


Fig. 2-21. On-board JTAG path for connection to external JTAG emulator.

TORNADO-P6x on-board JTAG-IN connector must be used for connection to either external JTAG emulator or to JTAG-OUT connector of previous JTAG device in JTAG path. On-board JTAG-OUT connector must be used in case another JTAG device(s) is(are) included in the same JTAG path after this particular *TORNADO-P6x* board. Refer to the corresponding subsections below for more details.

Using external JTAG emulator with single TORNADO-P6x board

In case external JTAG emulator is used for debugging single *TORNADO-P6x* board (fig. 2-22), then this emulator must connect to the dedicated on-board JTAG-IN connector (JP5) on *TORNADO-P6x* mainboard with JTAG-OUT connector (JP6) left unconnected, and on-board JTAG terminator (J4 jumper for *TORNADO-P62/P67* DSP systems, SW6-1 switch for *TORNADO-P6202/P6203* DSP systems, and SW4-4 switch for *TORNADO-P64xx* DSP systems) must be set to the 'ON' state (jumper must be installed). In this case JTAG path configuration file for TI C6000 Code Composer Studio IDE must be normally omitted (refer to TI C6000 Code Composer Studio IDE for details how to handle the JTAG path configuration file).

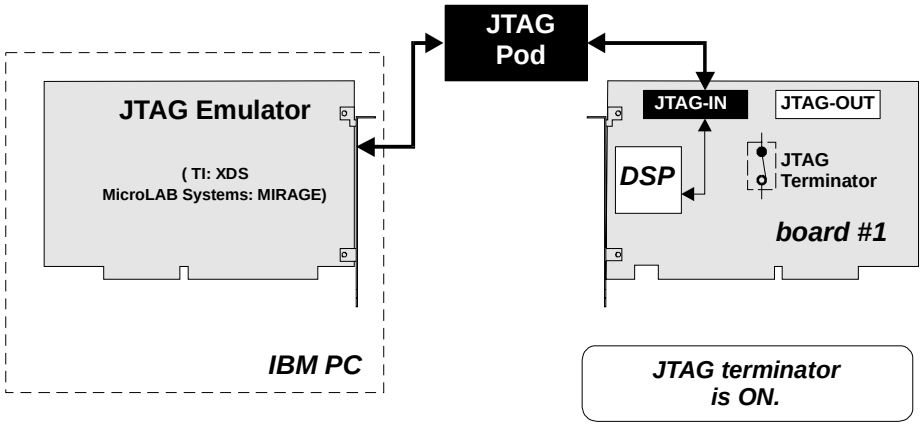


Fig. 2-22. Connection of external JTAG emulator to single *TORNADO-P6x* DSP system.

Using external JTAG emulator with multiple TORNADO-P6x boards

In case external JTAG emulator is used for debugging either multiple *TORNADO-P6x* DSP systems or *TORNADO-P6x* DSP system with other JTAG devices (other *TORNADO* DSP systems, FPGA, other DSP) in the same JTAG path, then this JTAG emulator must connect to *TORNADO-P6x* on-board JTAG-IN connector (JP5) of the first *TORNADO-P6x* board in this JTAG-path (fig. 2-23).

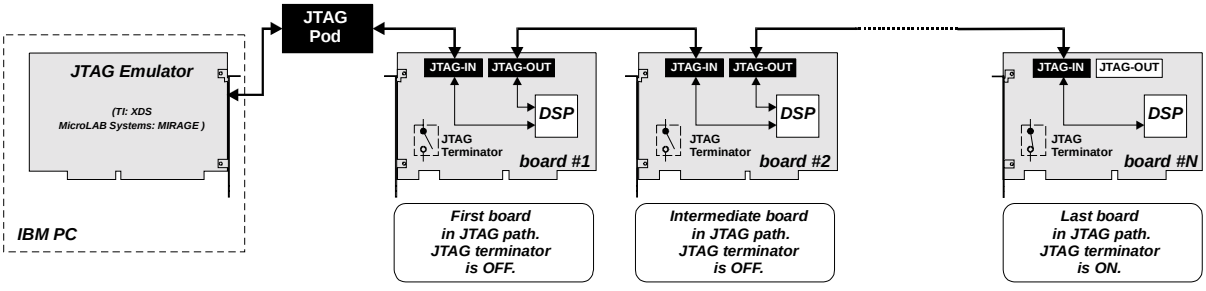


Fig. 2-23. Connection of external JTAG emulator to multiple *TORNADO-P6x* DSP system.

On-board JTAG-OUT connector(s) (JP6) of the first and intermediate *TORNADO-P6x* DSP systems shall connect to JTAG input connector(s) of the next JTAG device in JTAG path via JTAG EXTENSION CABLE (JTAG daisy-chaining). A variety of JTAG devices, which can be included together with *TORNADO-P6x* DSP system board into the same JTAG path, comprises of any JTAG compatible devices without any restrictions (digital logic, FPGA, other DSP, etc).

CAUTION

All *TORNADO-P6x* DSP systems in one multi-device JTAG path shall configure their on-board DSP JTAG multiplexer to connect to on-board JTAG-IN connector (JP5) instead of using the on-board *ECC* emulation controller. This configuration must be set via command line option *-ex* of *TP6CC.EXE* PC DOS software utility (or *TCC.EXE TSDK* Windows utility).

Last JTAG device in JTAG path must terminate JTAG path and return the JTAG *TDO* signal back to JTAG emulator, which is connected to the first JTAG device in JTAG path.

CAUTION

TORNADO-P62/P67 on-board J4 jumper, *TORNADO-P6202/P6203* on-board SW6-1 switch, *TORNADO-P64xx* on-board SW4-4 switch are used for termination of JTAG path on *TORNADO-P6x* DSP systems.

J4 jumper on *TORNADO-P62/P67* board, SW6-1 switch on *TORNADO-P6202/P6203* board, and SW4-4 switch on *TORNADO-P64xx* board shall be set to the 'ON' state (jumper must be installed) in case *TORNADO-P6x* is either the only or the last JTAG device in JTAG path.

J4 jumper on *TORNADO-P62/P67* board, SW6-1 switch on *TORNADO-P6202/P6203* board, and SW4-4 switch on *TORNADO-P64xx* board shall be set to the 'OFF' state (jumper must be removed) in case two or more JTAG devices are included into JTAG path, and this particular *TORNADO-P6x* DSP system is not the last JTAG device in this JTAG path.

CAUTION

In case *TORNADO-P6x* is used with other JTAG devices connected to on-board JTAG-OUT connector, then the next JTAG devices shall use JTAG default *TCK* clock source, which is the output from on-board JTAG-OUT connector of the fist *TORNADO-P6x* DSP system in this JTAG path.

In case there are two and more devices in JTAG path, then the debugger, which is used to debug particular JTAG devices in JTAG path, must accurately specify all JTAG devices exactly as they appear in this JTAG path in order to exclude JTAG processing errors. A list of JTAG devices and the order of their appearance in JTAG path shall be typically specified in debugger's JTAG configuration file (refer to TI C6000 Code Composer Studio IDE and other debuggers for details how to handle the JTAG path configuration file).

TORNADO-P6x on-board JTAG-path for ECC

In case *TORNADO-P6x* on-board JTAG path is configured to operate with on-board *ECC*, then the only difference with usage external JTAG emulator is that the on-board JTAG-IN connector (JP5) is excluded from JTAG path and is replaced by on-board *ECC* (fig.2-24). In this case the on-board JTAG path will comprise of on-board *ECC*, JTAG port of on-board TMS320C6x DSP and JTAG-OUT connector (JP6). *TORNADO-P6x* on-board JTAG terminator (J4 jumper for *TORNADO-P62/P67* DSP systems, SW6-1 switch for *TORNADO-P6202/P6203* DSP systems, and SW4-4 switch for *TORNADO-P64xx* DSP systems) must be used to terminate JTAG path in case this *TORNADO-P6x* board is either the last or the only JTAG device in JTAG path.

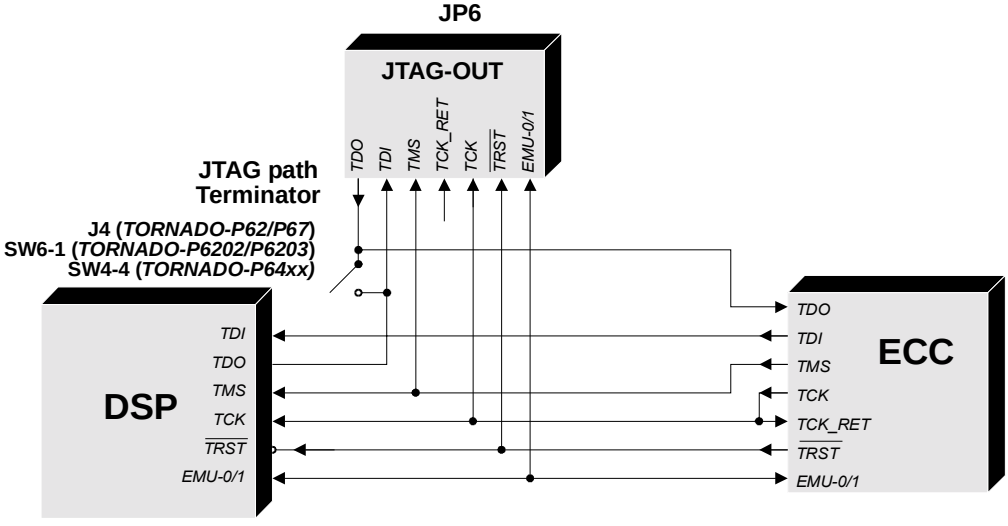


Fig. 2-24. TORNADO-P6x on-board JTAG path with *ECC*.

Using ECC for emulation of single TORNADO-P6x board

In case *TORNADO-P6x* on-board *ECC* is used for debugging one (this particular) *TORNADO-P6x* DSP system, then the on-board JTAG terminator (J4 jumper for *TORNADO-P62/P67* DSP systems, SW6-1 switch for *TORNADO-P6202/P6203* DSP systems, and SW4-4 switch for *TORNADO-P64xx* DSP systems) must be set to the 'ON' state (jumper must be installed) and JTAG-OUT connector (JP6) left unconnected (fig. 2-25). In this case JTAG path configuration file for TI C6000 Code Composer Studio IDE must be normally omitted (refer to TI C6000 Code Composer Studio IDE for details how to handle the JTAG path configuration file).

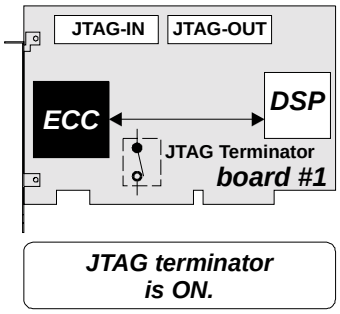


Fig. 2-25. JTAG path for debugging one *TORNADO-P6x* DSP system using on-board *ECC*.

Using ECC with multiple TORNADO-P6x boards

In case *TORNADO-P6x* on-board *ECC* is used for debugging either multiple *TORNADO-P6x* DSP systems or *TORNADO-P6x* DSP system with different JTAG device(s) (other *TORNADO* boards, FPGA, other DSP) in the same JTAG path, then this JTAG path will appear as shown at fig. 2-26.

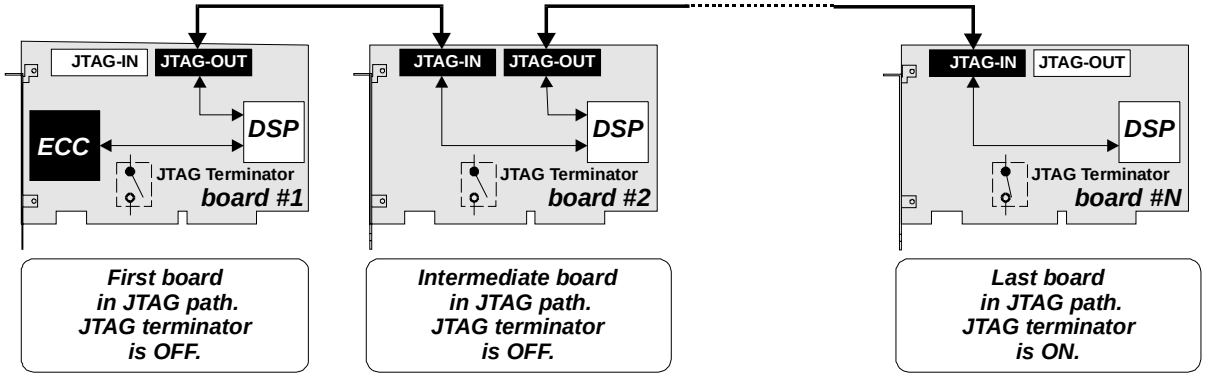


Fig. 2-26. Connection of multiple *TORNADO-P6x* boards to the *ECC* JTAG path.

TORNADO-P6x on-board JTAG-OUT connectors (JP6) of the first and intermediate *TORNADO-P6x* DSP systems shall connect to the next JTAG devices in JTAG path using JTAG EXTENSION CABLE in the daisy-chain manner.

CAUTION

All *TORNADO-P6x* DSP systems in one multi-device JTAG path shall configure their on-board DSP JTAG multiplexer to connect to on-board JTAG-IN connector (JP5) instead of using the on-board *ECC* emulation controller. This configuration must be set via command line option *-ex* of *TP6CC.EXE* PC DOS software utility (or *TCC.EXE TSDK* Windows utility).

Last JTAG device in JTAG path must terminate JTAG path and return the JTAG *TDO* signal back to JTAG emulator, which is connected to the first JTAG device in JTAG path.

CAUTION

TORNADO-P62/P67 on-board J4 jumper, *TORNADO-P6202/P6203* on-board SW6-1 switch, *TORNADO-P64xx* on-board SW4-4 switch are used for termination of JTAG path on *TORNADO-P6x* DSP systems.

J4 jumper on *TORNADO-P62/P67* board, SW6-1 switch on *TORNADO-P6202/P6203* board, and SW4-4 switch on *TORNADO-P64xx* board shall be set to the 'ON' state (jumper must be installed) in case *TORNADO-P6x* is either the only or the last JTAG device in JTAG path.

J4 jumper on *TORNADO-P62/P67* board, SW6-1 switch on *TORNADO-P6202/P6203* board, and SW4-4 switch on *TORNADO-P64xx* board shall be set to the 'OFF' state (jumper must be removed) in case two or more JTAG devices are included into JTAG path, and this particular *TORNADO-P6x* DSP system is not the last JTAG device in this JTAG path.

CAUTION

In case *TORNADO-P6x* is used with other JTAG devices connected to on-board JTAG-OUT connector, then the next JTAG devices shall use JTAG default *TCK* clock source, which is the output from on-board JTAG-OUT connector of the fist *TORNADO-P6x* DSP system in this JTAG path.

In case there are two and more devices in JTAG path, then the debugger, which is used to debug particular JTAG devices in JTAG path, must accurately specify all JTAG devices exactly as they appear in this JTAG path in order to exclude JTAG processing errors. A list of JTAG devices and the order of their appearance in JTAG path shall be typically specified in debugger's JTAG configuration file (refer to TI C6000 Code Composer Studio IDE and other debuggers for details how to handle the JTAG path configuration file).

2.7 Software Development Tools

TMS320C6x DSP is now an industry standard DSP and is supported by a variety of software development tools from multiple 3rd party vendors.

Compilers and Debuggers

Software development for *TORNADO-P6x* DSP systems is supported by TI TMS320C6x DSP Optimizing C Compiler and Assembly Language Tools.

Debugging of TMS320C6x DSP resident software for *TORNADO-P6x* is supported by TI C6000 Code Composer Studio IDE tools (www.ti.com), which require either external JTAG emulator (TI XDS or MicroLAB Systems *MIRAGE*) or on-board emulation controller chip (*ECC*).

Hypersignal RIDE Visual DSP Algorithm Development and Simulation Tool

TORNADO-P6x DSP systems are supported by DSP algorithm development tools from Hyperception Inc (www.hyperception.com), which include Hypersignal Block Diagram, RIDE and Code Generator, VAB and more.

Hypersignal RIDE is a visual real-time integrated DSP algorithm development and simulation environment for Windows 95/98/NT, and allows entry of DSP algorithm using high-level function blocks (FIR, FFT, math, etc). Entered DSP algorithm is compiled and loaded into *TORNADO-P6x* DSP system automatically during design procedure in order to evaluate the algorithm parameters for real-time execution and to benefit from the ultra-high performance of *TORNADO-P6x* DSP systems.

Real-time Multitasking Operating Systems (RTOS)

TORNADO-P6x is supported by multiple RTOS that provide multitasking capabilities:

- *DSP/BIOS* from Texas Instruments Inc (www.ti.com), which comes as the part of TI C6000 Code Composer Studio IDE
- *3L Diamond* from 3L Inc (www.3L.com) is an industry standard high-performance RTOS and provides full featured multitasking support for single-C6x and multi-C6x DSP applications.
- *NUCLEUS PLUS* from Accelerated Technology Inc (www.atinucleus.com) is an industry standard single-processor high-performance RTOS and provides full feature multitasking support. It features low cost and comes standard with source codes. Available options include *NUCLEUS FILE*, *NUCLEUS NET*, and *NUCLEUS DBUG+* that also come in source codes.

Application Software Tools for TORNADO-P6x

Application specific tools for *TORNADO-P6x* DSP system include a variety of function libraries for DSP, math, vector, image, etc computation, as well as function libraries for vocoder/fax/modem applications and audio multimedia.

Chapter 3. Installation and Configuration

This chapter includes instructions for configuration and installation of *TORNADO-P6x* DSP system into host PCI-bus PC.

3.1 Configuration and installation of *TORNADO-P6x* DSP System

Once you have unpacked *TORNADO-P6x* board, it is actually ready for installation into 32-bit PCI-bus slot of host PC. However it is recommended to follow the recommendation below in order to ensure that your *TORNADO-P6x* board is correctly configured:

- switch off power of host PC
- install SIOX and PIOX DCM into on-board SIOX and PIOX/PIOX-16 DCM sites
- configure the on-board DSP bootmode jumper (J1 jumper set on *TORNADO-P62/P67* DSP systems and SW2 switch on *TORNADO-P6202/P6203/P64xx* DSP systems) in accordance with tables 2-2a and 2-2b in order to meet requirements of your application
- configure TMS320C64xx DSP on-chip external peripheral (UTOPIA or McBSP-1) via on-board SW4-3 switch for *TORNADO-P6415/P6416* DSP systems in accordance with table 2-14 in order to meet requirements of your application
- configure SIO-0 port of on-board SIOX-A rev.B/C sites of *TORNADO-P6202/P6203/P64xx* DSP systems via on-board SW4-1 switch in accordance with table 2-27 (*TORNADO-P6202/P6203*) and table 2-29 (*TORNADO-P64xx*) in order to meet requirements of your application and technical specifications for installed SIOX-A rev.B/C DCM
- configure SIO-0 and SIO-1 ports of on-board SIOX-B rev.C site via J2 jumper set on *TORNADO-P62/P67* DSP systems and SW4-2 switch on *TORNADO-P6202/P6203/P64xx* DSP systems in accordance with table 2-26 (*TORNADO-P62/P67*), table 2-28 (*TORNADO-P6202/P6203*) and table 2-30 (*TORNADO-P64xx*) in order to meet requirements of your application and technical specifications for installed SIOX-B rev.C DCM
- configure DSP timer I/O (J5/J6 jumpers on *TORNADO-P62/P67* DSP systems, SW4-3/4 switches on *TORNADO-P6202/P6203* DSP systems, and SW5-1/2/3 switches on *TORNADO-P64xx* DSP systems) in accordance with figures 2-4a, 2-4b and 2-4c
- if it is required, install FLASH/EPROM chip into on-board socket S1 and configure on-board FLASH/EPROM type selector jumper (J3 jumper set on *TORNADO-P62/P67* DSP systems and SW3 switch on *TORNADO-P6202/P6203/P64xx* DSP systems) in accordance with table 2-5
- configure on-board JTAG terminator (J4 jumper on *TORNADO-P62/P67* DSP systems, SW6-1 switch on *TORNADO-P6202/P6203* DSP systems, and SW4-4 switch on *TORNADO-P64xx* DSP systems) in accordance with section 2.6
- if required, connect external JTAG emulator to on-board JP5 JTAG-IN connector in accordance with instructions in section 2.6
- if *TORNADO-P6x* DSP system is intended for use with host PC environment, then:
  - install *TORNADO-P6x* board into host PC PCI-bus slot,
  - screw the on-board *TORNADO-P6x* mounting bracket to the rear panel of host PC
  - safely switch on power of host PC, wait until PC operating system boots, and run either *TORNADO-P6x* host PC DOS utilities (for PC with DOS and Windows 9x only), or

TORNADO Software Development Kit (*TSDK*) utilities in order to ensure correct installation of *TORNADO-P6x* DSP system board

- if *TORNADO-P6x* DSP system is intended for use as stand-alone controller, then:
  - ❑ connect external power supply via on-board install JP10 connector
  - ❑ switch on external power supply.

3.2 Installation of FLASH/EPROM chip onto *TORNADO-P6x* DSP System

Installation of FLASH/EPROM chip (see fig.2-2 and fig.A-1) onto *TORNADO-P6x* board must be performed while host PC power is switched off.

CAUTION

TORNADO-P6x mainboard is designed to carry the 5v-only 128K/512Kx8 FLASH chips and 5v EPROM 128K..1Mx8 chips in PLCC-32 IC package.

Installation of other FLASH/EPROM chips than that specified in table 2-5 can result in damage of FLASH/EPROM chip and/or of *TORNADO-P6x* hardware.

CAUTION

You have to set the on-board J3 jumper set on *TORNADO-P62/P67* DSP systems and SW3 switch on *TORNADO-P6202/P6203* DSP systems in accordance with table 2-5 in order to meet installed FLASH/EPROM chip type.

Installation of FLASH/EPROM chip

In order to FLASH/EPROM into the *TORNADO-P6x* S1 on-board socket follow the recommendations below (see fig. 3-1):

- switch off power of host PC
- remove *TORNADO-P6x* board from host PC PCI-bus slot
- take FLASH/EPROM chip by your fingers in such way that its front (labeling) surface is turned at you
- adjust FLASH /EPROM chip to be parallel to the surface of S1 PLCC-32 socket on *TORNADO-P6x* board
- orient FLASH/EPROM chip in such way, that the key corner of PLCC-32 IC package would match the corresponding corner of on-board S1 PLCC-32 IC socket
- safely insert FLASH/EPROM chip into on-board S1 PLCC-32 IC socket
- safely plug and fix FLASH/EPROM chip in on-board S1 PLCC-32 IC socket

- set J3 jumper set on *TORNADO-P62/P67* DSP systems and SW3 switch on *TORNADO-P6202/P6203* DSP systems in accordance with table 2-5 in order to meet installed FLASH/EPROM chip type
- install *TORNADO-P6x* board into host PCI-bus slot of host PC
- switch on power of host PC

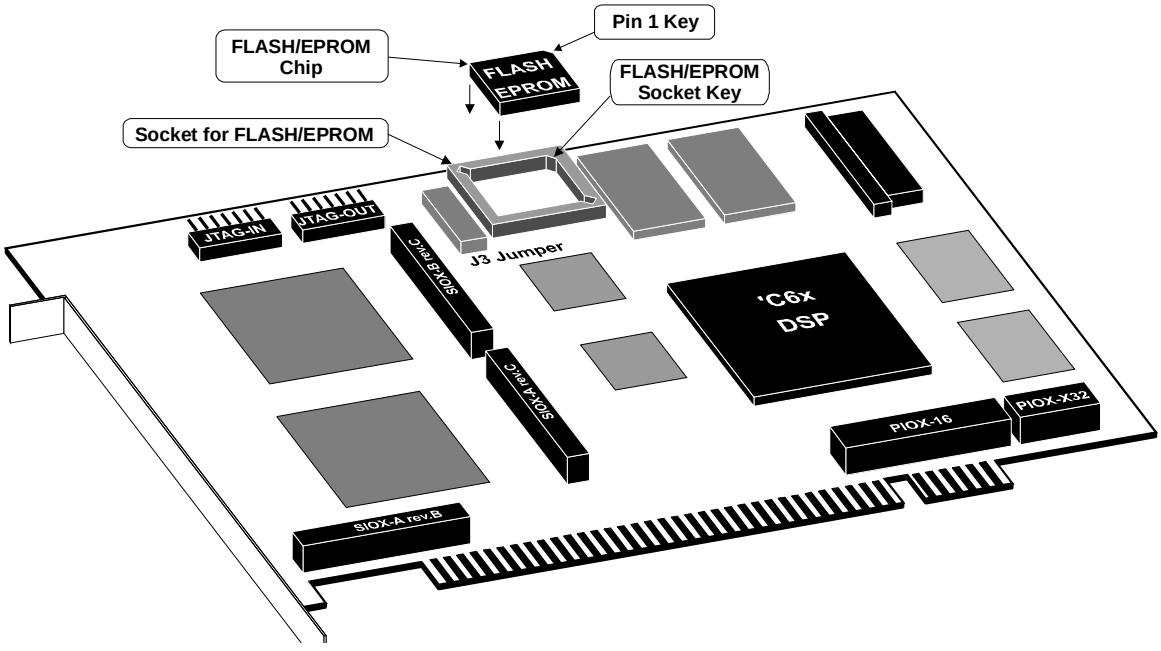


Fig.3-1. Installation of FLASH/EPROM chip onto *TORNADO-P6x* mainboard.

3.3 Using TI C6000 Code Composer Studio IDE tools with *TORNADO-P6x* DSP Systems

There are several minor options, which user must keep in mind when using TI C6000 Code Composer Studio IDE tools with *TORNADO-P6x* DSP systems.

TMS320C6x DSP reset control during running JTAG debugger

TORNADO-P6x on-board TMS320C6x DSP must be released from the 'RESET' state and placed into the 'RUN' state prior running TI C6000 Code Composer Studio IDE JTAG debugging tools.

CAUTION

It is not allowed to reset *TORNADO-P6x* on-board TMS320C6x DSP during active JTAG debugger session when running TI C6000 Code Composer IDE debugging tools. Violation of this requirement can result in hanging of TI C6000 Code Composer IDE debugger and may require debugger restart.

It case *TORNADO-P6x* on-board TMS320C6x DSP is running is host PC mode, then it can be released from the 'RESET' state via *TP6CC.EXE* host PC DOS software utility (or *TCC.EXE TSDK* Windows utility) using the following command line option:

TP6CC.EXE –cr0
TCC.EXE –cr0

It is recommended to reset *TORNADO-P6x* host PCI-bus interface and on-board DSP environment just after the host PC power on and after any DSP software trouble condition. This will guarantee that on-board DSP will be put into known state after DSP will be released from the 'RESET' state prior running TI C6000 Code Composer Studio IDE. Reset of *TORNADO-P6x* host PCI-bus interface and of on-board DSP environment can be done using *TP6CC.EXE* PC DOS software utility (or *TCC.EXE TSDK* Windows utility) with the *-r* and *–r –cr0* command line option:

TP6CC.EXE –r –cr0
TCC.EXE –r –cr0

In case *TORNADO-P6x* on-board DSP in running stand-alone mode, then either on-board SW1 DSP reset pushbutton must be pressed or active external DSP reset signal must be applied during start of JTAG debugger session of TI C6000 Code Composer IDE debugging tools. This will guarantee that on-board DSP on-board DSP will be in the known state during debugger initialization. However, DSP reset signal must be immediately removed after JTAG debugger of TI C6000 Code Composer Studio IDE tools will initialize successfully.

Debugging TMS320C6x DSP via external JTAG emulator

In cased external JTAG emulator is considered to be used for debugging *TORNADO-P6x* on-board DSP, then *TORNADO-P6x* on-board JTAG multiplexer must be configured to connect to on-board JTAG-IN connector (JP5) instead of using the on-board *ECC* emulation controller. This configuration can be set via *TP6CC.EXE* PC DOS software utility (or *TCC.EXE TSDK* Windows utility) as the following:

TP6CC.EXE –ex
TCC.EXE –ex

Debugging TMS320C6x DSP via on-board ECC emulation controller

In cased on-board *ECC* emulation controller is considered to be used for debugging *TORNADO-P6x* on-board DSP, then the *TP6XNT.DVR* driver for *TORNADO-P6x* on-board *ECC* emulation controller for TI C6000 Code Composer Studio IDE debugging tools must be installed and selected as the primary emulator driver via Code Composer Studio Setup utility.

CAUTION

TP6XNT.DVR driver for *TORNADO-P6x* on-board *ECC* emulation controller for TI C6000 Code Composer Studio IDE debugging tools comes standard with *TORNADO-P6x* DSP system shipment kit and is available upon request from MicroLAB Systems.

In cased on-board *ECC* emulation controller is considered to be used for debugging *TORNADO-P6x* on-board DSP, then *TORNADO-P6x* on-board JTAG multiplexer must be configured to connect to on-board *ECC* instead of on-board JTAG-IN connector (JP5). This configuration can be set via *TP6CC.EXE* PC DOS software utility (or *TCC.EXE TSDK* Windows utility) as the following:

TP6CC.EXE –ei -er
TCC.EXE –ei -er

Chapter 4. Utility Software

This chapter contains description of PC DOS utility software for *TORNADO-P6x* DSP systems, which runs under DOS v.3.x and later and Windows 95/98 only. Described utilities are platform specific, i.e. they run with *TORNADO-P6x* DSP systems only.

MicroLAB Systems also provides *TORNADO Software Development Kit (TSDK)* universal host programming API for *TORNADO* DSP systems and controllers. *TSDK* runs under for Windows 95/98/NT/2000/XP platforms, provides similar utilities, and is not *TORNADO* platform specific.

CAUTION

This manual does not contain description for *TORNADO Software Development Kit (TSDK)* host PC software for Windows 95/98/NT/2000/XP for *TORNADO* DSP systems and controllers. Refer to *TSDK* user's guide for more details.

TSDK comes standard with all *TORNADO* DSP systems and controllers, and is available upon request from MicroLAB Systems.

CAUTION

TORNADO-P6x host PC DOS utilities (including *TP6CC.EXE* and *TP6COFF.EXE* software utilities) support allocation of DPRAM area of *TORNADO-P64xx* host PCI-bus interface to PCI-bus UMB memory area (below 1 Mbyte) only, which can be set via *TP_DP1M.EXE* host PC DOS utility (requires reboot of host PC).

CAUTION

TORNADO-P6x host PC DOS utilities (including *TP6CC.EXE* and *TP6COFF.EXE* software utilities) support alternative DPRAM area configuration for *TORNADO-P64xx* host PCI-bus interface with direct mapping of 32 kbyte sub-area of on-board DPRAM memory to PCI-bus UMB memory area (below 1 Mbyte) only.

Alternative DPRAM area configuration for *TORNADO-P64xx* host PCI-bus interface can be set via *TP_DP1M.EXE* host PC DOS utility (requires reboot of host PC).

Alternative DPRAM area configuration for *TORNADO-P64xx* host PCI-bus interface is not supported by *TSDK* software for Windows.

4.1 *TP6CC.EXE* Control Center PC DOS Utility

TP6CC.EXE ("*TORNADO-P6x* Control Center") PC DOS utility is a DOS command line control software tool for *TORNADO-P6x* that delivers easy and powerful user control for *TORNADO-P6x* hardware. *TP6CC.EXE* utility provides the following functionality:

- display/set PCI operation registers of S5933 PCIC area of host PCI-bus interface
- display/set HIF registers of *TORNADO-P6x* host PCI-bus interface
- read/write to all DPRAM memory and all DPSEM dual-port hardware semaphores via DPRAM/DPSEM area of host PCI-bus interface for *TORNADO-P62xx/P67* DSP systems
- read/write to 32 kbyte DPRAM memory sub-area, which is allocated to DPRAM area of host PCI-bus interface for *TORNADO-P64xx* DSP systems
- read/write to all TMS320C6x DSP memory areas via the DSP on-chip HPI port
- configure on-board DSP JTAG multiplexer and initialize *ECC* emulation controller.

CAUTION

TP6CC.EXE host PC DOS utility assumes that on-board TMS320C620x/C6701 DSP of *TORNADO-P62xx/P67* DSP is configured to start in '*NO BOOT*' DSP bootmode via on-board jumpers and switches. Refer to table 2-2 for more details.

On-board DSP bootmode switch setting for *TORNADO-P64xx* DSP systems has no meaning for *TP6CC.EXE* host PC DOS utility.

TP6CC.EXE utility must be invoked from DOS prompt with up to ten command line options:

TP6CC [*-option1*] [*-option2*] [*-option3*] ...

Each command line option corresponds to specific *TORNADO-P6x* hardware control operation. The following is a list of available command line options for *TP6CC.EXE* utility.

Options for access to HIF_CONTROL_RG register

-hc	Display contents of *HIF_CONTROL_RG* register.
-hc0	Clear contents of *HIF_CONTROL_RG* register.
-hcr	Display current state of DSP host reset signal, which is defined by *M_GO* bit of *HIF_CONTROL_RG* register.
-hcr0	Release DSP reset signal, i.e. put DSP into the RUN state. This option sets *M_GO* bit of *HIF_CONTROL_RG* register to the logical '1' state in case *M_SA_MODE* bit is set to '0'.
-hcr1	Set active DSP reset signal, i.e. put DSP into the RESET state. This option clears *M_GO* bit of *HIF_CONTROL_RG* register in case *M_SA_MODE* bit is set to '0'.
-hcsa	Display current state of DSP operation mode, which is defined by *M_SA_MODE* bit of *HIF_CONTROL_RG* register.

-hcsa0	Set DSP host reset control mode. This option clears *M_SA_MODE* bit of *HIF_CONTROL_RG* register.
-hcsa1	Set DSP host reset control mode. This option sets *M_SA_MODE* bit of *HIF_CONTROL_RG* register to the logical '1' state.
-hcam	Display current state of DSP PCI-bus mastering enable, which is defined by *AM_EN* bit of *HIF_CONTROL_RG* register.
-hcam0	Disable DSP PCI-bus mastering. This option clears *AM_EN* bit of *HIF_CONTROL_RG* register.
-hcam1	Enable DSP PCI-bus mastering. This option sets *AM_EN* bit of *HIF_CONTROL_RG* register to the logical '1' state.
-hcdsr	Display current state of *DSP_M_GO* bit of *HIF_CONTROL_RG* register.
-hcdsp	Display current state of *DSP_PD* bit of *HIF_CONTROL_RG* register.

Options for access to HIF_IM_RG Interrupt Mask register

-him	Display contents of *HIF_IM_RG* register.
-him0	Clear contents of *HIF_IM_RG* register.
-himde	Display current state of *DPRAM_ERR_IE* bit (AOB host interrupt enable on DPRAM access timeout error) of *HIF_IM_RG* register (*TORNADO-P62xx/P67* only).
-himde0	Clear *DPRAM_ERR_IE* bit of *HIF_IM_RG* register and disable AOB host interrupts on DPRAM access timeout error (*TORNADO-P62xx/P67* only).
-himde1	Set *DPRAM_ERR_IE* bit of *HIF_IM_RG* register to the logical '1' state and enable AOB host interrupts on DPRAM access timeout error (*TORNADO-P62xx/P67* only).
-himdi	Display current state of *PCI_DPRAM_IRQ_IE* bit (AOB host interrupt enable on DSP-to-PCI interrupt request via DPRAM) of *HIF_IM_RG* register (*TORNADO-P62xx/P67* and *TORNADO-P64xx* with 256Kx32 DPRAM only).
-himdi0	Clear *PCI_DPRAM_IRQ_IE* bit of *HIF_IM_RG* register and disable AOB host interrupts on DSP-to-PCI interrupt request via DPRAM (*TORNADO-P62xx/P67* and *TORNADO-P64xx* with 256Kx32 DPRAM only).
-himdi1	Set *PCI_DPRAM_IRQ_IE* bit of *HIF_IM_RG* register to the logical '1' state and enable AOB host interrupts on DSP-to-PCI interrupt request via DPRAM (*TORNADO-P62xx/P67* and *TORNADO-P64xx* with 256Kx32 DPRAM only).
-himhe	Display current state of *HPI_ERR_IE* bit (AOB host interrupt enable on DSP HPI access timeout error) of *HIF_IM_RG* register.
-himhe0	Clear *HPI_ERR_IE* bit of *HIF_IM_RG* register and disable AOB host interrupts on DSP HPI access timeout error.

-himhe1 Set *HPI_ERR_IE* bit of *HIF_IM_RG* register to the logical '1' state and enable AOB host interrupts on DSP HPI access timeout error.

-himhi Display current state of *HPI_HINT_IE* bit (AOB host interrupt enable on DSP-to-PCI interrupt request via DSP HPI) of *HIF_IM_RG* register (*TORNADO-P62/P67/P64xx* DSP systems only).

-himhi0 Clear *HPI_HINT_IE* bit of *HIF_IM_RG* register and disable AOB host interrupts on DSP-to-PCI interrupt request via DSP HPI (*TORNADO-P62/P67/P64xx* DSP systems only).

-himhi1 Set *HPI_HINT_IE* bit of *HIF_IM_RG* register to the logical '1' state and enable AOB host interrupts on DSP-to-PCI interrupt request via DSP HPI (*TORNADO-P62/P67/P64xx* DSP systems only).

-himm Display current state of *MH_RQ_IE* bit (AOB host interrupt enable on DSP-to-PCI interrupt request via *DSP_MH_RQ_RG* IOX register) of *HIF_IM_RG* register.

-himm0 Clear *MH_RQ_IE* bit of *HIF_IM_RG* register and disable AOB host interrupts on DSP-to-PCI interrupt request via *DSP_MH_RQ_RG* IOX register.

-himm1 Set *MH_RQ_IE* bit of *HIF_IM_RG* register to the logical '1' state and enable AOB host interrupts on DSP-to-PCI interrupt request via *DSP_MH_RQ_RG* IOX register.

Options for access to HIF_IS_RG Interrupt Status register

-his Display contents of *HIF_IS_RG* register.

-hisde Display current state of *DPRAM_ERR* bit (AOB host interrupt request on DPRAM access timeout error) of *HIF_IS_RG* register (*TORNADO-P62xx/P67* only).

-hisde0 Clear *DPRAM_ERR* bit of *HIF_IS_RG* register (*TORNADO-P62xx/P67* only).

-hisdi Display current state of *PCI_DPRAM_IRQ* bit (AOB host interrupt request on DSP-to-PCI interrupt request via DPRAM) of *HIF_IS_RG* register (*TORNADO-P62xx/P67* and *TORNADO-P64xx* with 256Kx32 DPRAM only).

-hishe Display current state of *HPI_ERR* bit (AOB host interrupt request on DSP HPI access timeout error) of *HIF_IS_RG* register.

-hishe0 Clear *HPI_ERR* bit of *HIF_IS_RG* register.

-hishi Display current state of *HPI_HINT* bit (AOB host interrupt request on DSP-to-PCI interrupt request via DSP HPI) of *HIF_IS_RG* register (*TORNADO-P62/P67/P64xx* DSP systems only).

-hism	Display current state of *MH_RQ* bit (AOB host interrupt request on DSP-to-PCI interrupt request via *DSP_MH_RQ_RG* IOX register) of *HIF_IS_RG* register.
-hism0	Clear *MH_RQ* bit of *HIF_IM_RG* register.

Options for access to HIF_HM_RQ0_RG and HIF_HM_RQ1_RG PCI-to-DSP Interrupt Request registers

-hhm	Display current contents of both *HIF_HM_RQ0_RG* and *HIF_HM_RQ1_RG* registers, which are used for generation of PCI-to-DSP interrupt requests *HM_RQ0* and *HM_RQ1*.
-hhm0	Display current contents of *HIF_HM_RQ0_RG* register, which is used for generation of PCI-to-DSP interrupt request *HM_RQ0*.
-hhm0,D	Write 4-bit hex value *D* to *HIF_HM_RQ0_RG* register and generate PCI-to-DSP interrupt request *HM_RQ0*.
-hhm1	Display current contents of *HIF_HM_RQ1_RG* register, which is used for generation of PCI-to-DSP interrupt request *HM_RQ1*.
-hhm1,D	Write 4-bit hex value *D* to *HIF_HM_RQ1_RG* register and generate PCI-to-DSP interrupt request *HM_RQ1*.

Options for access to HIF_DSP_BMODE_RG DSP Bootmode register (TORNADO-P64xx only)

-hb	Display current DSP bootmode (*TORNADO-P64xx* only).
-hbn	Set DSP bootmode to '*NO BOOT*' (*TORNADO-P64xx* only). This option has effect only in case *TORNADO-P64xx* DSP is running in host PC operation mode and is in the 'RESET' state.
-hbh	Set DSP bootmode to '*HPI BOOT*' (*TORNADO-P64xx* only). This option has effect only in case *TORNADO-P64xx* DSP is running in host PC operation mode and is in the 'RESET' state.
-hbf	Set DSP bootmode to '*FLASH BOOT*' (*TORNADO-P64xx* only). This option has effect only in case *TORNADO-P64xx* DSP is running in host PC operation mode and is in the 'RESET' state.

Options for DPRAM/DPSEM access

-da	Display contents of *HIF_SMP0_RG* and *HIF_SMP1_RG* registers, which define area, DPRAM page number, and dual/single-page access mode to the DPRAM/DPSEM area, which will be used during host PCI-bus access to the DPRAM/DPSEM area (*TORNADO-P62xx/P67* only).
-ddp0	Set /single-page access mode to the DPRAM/DPSEM area (*TORNADO-P62xx/P67* only).
-ddp1	Set dual-page access mode to the DPRAM/DPSEM area (*TORNADO-P62xx/P67* only).

-da0lA@Z Configure *HIF_SMP0_RG* register to access the *Z* area ('M' - for DPRAM area, 'S' - for DPSEM area) and DPRAM/DPSEM dataword at *A* hex address (*TORNADO-P62xx/P67* only).

-da1lA@Z Configure *HIF_SMP1_RG* (N=1) register to access the *Z* area ('M' - for DPRAM area, 'S' - for DPSEM area) and DPRAM/DPSEM dataword at *A* hex address (*TORNADO-P62xx/P67* only).

-dmdSA,EA Display 32-bit DPRAM data words starting from the *SA* start address and up to the *EA* end address. *HIF_SMP0_RG* register will be used for access to the DPRAM/DPSEM area, and the contents of *HIF_SMP0_RG* register will be restored on exit (*TORNADO-P62xx/P67* only). (For *TORNADO-P64xx* DSP systems, specified address must be within 00000000H..00007FFFH address range)

-dmdSA,EA@b Display 8-bit DPRAM data words (bytes) starting from the *SA* start address and up to the *EA* end address. *HIF_SMP0_RG* register will be used for access to the DPRAM/DPSEM area, and the contents of *HIF_SMP0_RG* register will be restored on exit (*TORNADO-P62xx/P67* only). (For *TORNADO-P64xx* DSP systems, specified address must be within 00000000H..00007FFFH address range)

-dmdSA,EA@h Display 16-bit DPRAM data words starting from the *SA* start address and up to the *EA* end address. *HIF_SMP0_RG* register will be used for access to the DPRAM/DPSEM area, and the contents of *HIF_SMP0_RG* register will be restored on exit (*TORNADO-P62xx/P67* only). (For *TORNADO-P64xx* DSP systems, specified address must be within 00000000H..00007FFFH address range)

-dmwA,D Write 32-bit *D* hex data word to the DPRAM hex address *A*. *HIF_SMP0_RG* register will be used for access to the DPRAM/DPSEM area, and the contents of *HIF_SMP0_RG* register will be restored on exit (*TORNADO-P62xx/P67* only). (For *TORNADO-P64xx* DSP systems, specified address must be within 00000000H..00007FFFH address range)

-dmwA,D@b Write 8-bit *D* hex data word (byte) to the DPRAM hex address *A*. *HIF_SMP0_RG* register will be used for access to the DPRAM/DPSEM area, and the contents of *HIF_SMP0_RG* register will be restored on exit (*TORNADO-P62xx/P67* only). (For *TORNADO-P64xx* DSP systems, specified address must be within 00000000H..00007FFFH address range)

-dmwA,D@h Write 16-bit *D* hex data word to the DPRAM hex address *A*. *HIF_SMP0_RG* register will be used for access to the DPRAM/DPSEM area, and the contents of *HIF_SMP0_RG* register will be restored on exit (*TORNADO-P62xx/P67* only). (For *TORNADO-P64xx* DSP systems, specified address must be within 00000000H..00007FFFH address range)

-dmhm Display 32-bit contents of the DPRAM memory location, which is used for generation of PCI-to-DSP request via DPRAM (*DPRAM_HM_RQ*). *HIF_SMP0_RG* register will be used for access to the DPRAM/DPSEM area, and the contents of *HIF_SMP0_RG* register will be restored on exit

(*TORNADO-P62xx/P67* only). (*TORNADO-P62xx/P67* and *TORNADO-P64xx* with 256Kx32 DPRAM only)

-dmhmD — Write 32-bit hex value *D* to the DPRAM memory location, which is used for generation of PCI-to-DSP request via DPRAM (*DPRAM_HM_RQ*). *HIF_SMP0_RG* register will be used for access to the DPRAM/DPSEM area, and the contents of *HIF_SMP0_RG* register will be restored on exit (*TORNADO-P62xx/P67* only). (*TORNADO-P62xx/P67* and *TORNADO-P64xx* with 256Kx32 DPRAM only)

-dmmh — Display 32-bit contents of the DPRAM memory location, which is used for generation of DSP-to-PCI request via DPRAM (*DPRAM_MH_RQ*). *HIF_SMP0_RG* register will be used for access to the DPRAM/DPSEM area, and the contents of *HIF_SMP0_RG* register will be restored on exit (*TORNADO-P62xx/P67* only). (*TORNADO-P62xx/P67* and *TORNADO-P64xx* with 256Kx32 DPRAM only)

-dmmhD — Write 32-bit hex value *D* to the DPRAM memory location, which is used for generation of DSP-to-PCI request via DPRAM (*DPRAM_MH_RQ*). *HIF_SMP0_RG* register will be used for access to the DPRAM/DPSEM area, and the contents of *HIF_SMP0_RG* register will be restored on exit (*TORNADO-P62xx/P67* only). (*TORNADO-P62xx/P67* and *TORNADO-P64xx* with 256Kx32 DPRAM only)

-dsd — Display contents of all DPSEM hardware semaphores. *HIF_SMP0_RG* register will be used for access to the DPRAM/DPSEM area, and the contents of *HIF_SMP0_RG* register will be restored on exit. (*TORNADO-P62xx/P67* only)

-dsdN — Display contents of N-th DPSEM hardware semaphore. *HIF_SMP0_RG* register will be used for access to the DPRAM/DPSEM area, and the contents of *HIF_SMP0_RG* register will be restored on exit. (*TORNADO-P62xx/P67* only)

-dswN,D — Set N-th DPSEM hardware semaphore to hex *D* value (*D* value must be either ‘0’ or ‘1’). *HIF_SMP0_RG* register will be used for access to the DPRAM/DPSEM area, and the contents of *HIF_SMP0_RG* register will be restored on exit. (*TORNADO-P62xx/P67* only)

Options for the DSP HPI access

-hpic — Display contents of HPIC register of TMS320C6x DSP (*TORNADO-P62/P67/P64xx* DSP systems only).

-hpich0 — Clear *HINT* bit (DSP-to-PCI interrupt request via HPI) of HPIC register of TMS320C6x DSP (*TORNADO-P62/P67/P64xx* DSP systems only).

-hpidi — Display current state of *DSPINT* bit (PCI-to-DSP interrupt request via HPI) of TMS320C6201/C6701/C64xx DSP on-chip HPIC register for *TORNADO-P62/P67/P64xx* DSP systems and *DSPINT* bit of TMS320C6202/C6203 DSP on-chip XBISA (HPIA) register for *TORNADO-P6202/P6203* DSP systems.

-hpidi1 (-hpicd1) Set *DSPINT* bit (PCI-to-DSP interrupt request via HPI) of TMS320C6201/C6701/C64xx DSP on-chip HPIC register for *TORNADO-P62/P67/P64xx* DSP systems and *DSPINT* bit of TMS320C6202/C6203 DSP on-chip XBISA (HPIA) register for *TORNADO-P6202/P6203* DSP systems.

-hpidSA,EA Display 32-bit data words within the *SA...EA* hex HPI address range of TMS320C6x DSP.

-hpiwA,D Write 32-bit *D* hex data word at *A* hex HPI memory address of TMS320C6x DSP.

Options for access to PCI operation registers of S5933 PCIC

-pom Display contents/status of all PCI-to-DSP outgoing mailboxes *#0..#3* of S5933 PCIC, i.e. registers *PCIC_OMBX0_RG..PCIC_OMBX3_RG* .

-pomN Display contents/status of PCI-to-DSP outgoing mailbox *#N* (*N*=0..3) of S5933 PCIC, i.e. register *PCIC_OMBXn_RG*.

-pomN,D Write 32-bit hex value *D* to the PCI-to-DSP outgoing mailbox *#N* (*N*=0..3) of S5933 PCIC, i.e. register *PCIC_OMBXn_RG*.

-pim Display contents/status of all DSP-to-PCI incoming mailboxes *#0..#3* of S5933 PCIC, i.e. registers *PCIC_IMBXx_RG..PCIC_IMBX3_RG*.

-pimN Display contents/status of DSP-to-PCI incoming mailbox *#N* (*N*=0..3) of S5933 PCIC, i.e. register *PCIC_IMBXn_RG*.

-pf Display contents/status DSP-to-PCI FIFO of S5933 PCIC, i.e. register *PCIC_FIFO_RG*.

-pfD Write 32-bit hex value *D* to PCI-to-DSP FIFO of S5933 PCIC, i.e. register *PCIC_FIFO_RG*.

-pmbef Display contents of MBEF PCI operation register of S5933 PCIC, i.e. register *PCIC_MBEF_RG*.

-pintcsr Display contents of INTCSR PCI operation register of S5933 PCIC, i.e. register *PCIC_INTCSR_RG*.

-pintcsrD Write 32-bit hex value *D* to the INTCSR PCI operation register of S5933 PCIC, i.e. register *PCIC_INTCSR_RG*.

-pmcsr Display contents of MCSR PCI operation register of S5933 PCIC, i.e. register *PCIC_MCSR_RG*.

-pmcsrD Write 32-bit hex value *D* to the MCSR PCI operation register of S5933 PCIC, i.e. register *PCIC_MCSR_RG*.

-pmw Display contents of MWAR and MWTC PCI operation registers of S5933 PCIC, i.e. registers *PCIC_MWAR_RG* and *PCIC_MWTC_RG*, which correspond to the DSP-to-PCI transfers using PCI-bus mastering from the DSP environment.

-pmr Display contents of MRAR and MRTC PCI operation registers of S5933 PCIC, i.e. registers *PCIC_MRAR_RG* and *PCIC_MRTC_RG*, which correspond to the PCI-to-DSP transfers using PCI-bus mastering from the DSP environment.

Options for ECC control

-e Display current emulator source for *TORNADO-P6x* on-board JTAG path.

-ei Configure *TORNADO-P6x* on-board JTAG path to operate from on-board *ECC* and ignore external JTAG emulator via on-board JTAG-IN connector.

-ex Configure *TORNADO-P6x* on-board JTAG path to operate from external JTAG emulator via on-board JTAG-IN connector (on-board *ECC* is ignored).

-er Perform software reset of on-board *ECC*. This is the recommended operation prior running the TI C6000 Code Composer Studio IDE.

General options

-r Perform software reset of *TORNADO-P6x* host PCI-bus interface. All registers of host PCI-bus interface will be set into default states, the *ECC* chip is reset, DSP is put to the RESET state, all error flags are reset, and all host interrupt enable masks are reset. Also, the <B 0x00000000> program code will be written into the reset vector location of DSP interrupt table (default address 0x00000000 after DSP reset), which will guarantee that DSP will be put into known state after the DSP reset line will be released prior running the TI C6000 Code Composer Studio IDE via DSP on-chip JTAG port.

Board selection options

-ih Display PCI-bus allocation information for host PCI-bus interface of default *TORNADO-P6x* board.

-i62hN (-i2hN) Select *TORNADO-P62* board with the PCI-bus index *#N* (*N* must be a decimal value within the 0..31 range).

-i67hN (-i7hN) Select *TORNADO-P67* board with the PCI-bus index *#N* (*N* must be a decimal value within the 0..31 range).

-i6202hN Select *TORNADO-P6202* board with the PCI-bus index *#N* (*N* must be a decimal value within the 0..31 range).

-i6203hN Select *TORNADO-P6203* board with the PCI-bus index *#N* (*N* must be a decimal value within the 0..31 range).

-i6414hN Select *TORNADO-P6414* board with the PCI-bus index *#N* (*N* must be a decimal value within the 0..31 range).

-i6415hN Select *TORNADO-P6415* board with the PCI-bus index *#N* (*N* must be a decimal value within the 0..31 range).

-i6416hN Select *TORNADO-P6416* board with the PCI-bus index *#N* (*N* must be a decimal value within the 0..31 range).

Utility options

-p Set page-by-page display mode. Pressing "ESC" key will terminate display output, whereas pressing any other key will result in the next page display.

-? Display list of available options for *TP6CC.EXE* utility program. Help list is also displayed when *TP6CC.EXE* utility program is invoked without command line options.

CAUTION

In case no board selection option is specified for *TP6CC.EXE* software utility, then default *TORNADO-P6x* board will be selected as the following:
TORNADO-P62 board with index #0 will be selected as default in case it presents, otherwise *TORNADO-P67* board with index #0 will be selected as default in case it presents, otherwise *TORNADO-P6202* board with index #0 will be selected as default in case it presents, otherwise *TORNADO-P6203* board with index #0 will be selected as default in case it presents, otherwise *TORNADO-P6414* board with index #0 will be selected as default in case it presents, otherwise *TORNADO-P6415* board with index #0 will be selected as default in case it presents, otherwise *TORNADO-P6416* board with index #0 will be selected as default in case it presents.

4.2 Uploading TMS320C6x COFF-files via Host PCI-bus Interface using *TP6COFF.EXE* PC DOS Utility

Uploading of TI TMS320C6x COFF-files (output .OUT files of TI TMS320C6x C/Assembler tools) into *TORNADO-P6x* on-board TMS320C6x DSP environment (DPRAM, SBSRAM, SDRAM, DSP on-chip areas, etc) can be performed by means of *TP6COFF.EXE* PC DOS software utility, which is included with *TORNADO-P6x* PC DOS utility software. *TP6COFF.EXE* utility loads TI TMS320C6x COFF-file into *TORNADO-P6x* environment via host PCI-bus interface and does not use the on-board emulation controller *ECC*.

CAUTION

TP6COFF.EXE host PC DOS utility assumes that on-board TMS320C620x/C6701 DSP of *TORNADO-P62xx/P67* DSP is configured to start in '*NO BOOT*' DSP bootmode via on-board jumpers and switches. Refer to table 2-2 for more details.

On-board DSP bootmode switch setting of *TORNADO-P64xx* DSP systems has no meaning for *TP6COFF.EXE* host PC DOS utility.

The following data upload modes are supported when uploading COFF-file into the *TORNADO-P6x* environment:

- *standard mode*, i.e. in case *TORNADO-P6x* on-board DSP is in the 'RUN' state and data is uploaded to on-board DPRAM area only of host PCI-bus interface for *TORNADO-P62xx/P67* DSP systems and to any DSP memory area for *TORNADO-P64xx* DSP systems
- *reset mode*, i.e. when data is uploaded to all TMS320C6x DSP memory areas via host PCI-bus interface using DSP reset control.

Standard mode is used to upload of COFF-file to the DPRAM area only for *TORNADO-P62xx/P67* DSP systems while on-board DSP is in the 'RUN' state, and does not allow to upload data to the TMS320C6x DSP environment areas, which are not directly accessible via host PCI-bus interface (SBSRAM, SDRAM, DSP on-chip areas, etc). This mode is useful for run-time data upload via DPRAM of *TORNADO-P62xx/P67* DSP systems while DSP is executing the program and even while other host PC environment is communicating with the DSP. For *TORNADO-P62xx/P67* DSP systems, this mode allows to upload COFF-file data to all DSP memory areas via DSP on-chip HPI port while on-board DSP is in the 'RUN' state. This upload mode does not alter DSP reset control.

Reset mode provides upload of COFF-file to all TMS320C6x DSP environment areas including those, which are not directly accessible via host PCI-bus interface (SBSRAM, SDRAM, DSP on-chip areas, etc). This upload mode is default mode for *TP6COFF.EXE* software utility, and DSP reset control is used in this mode.

Uploading of COFF-file into *TORNADO-P6x* is performed by invoking *TP6COFF.EXE* utility from DOS command line:

TP6COFF FILENAME[.OUT] [*-option1*] [*-option2*] [*-option3*] *...*

If file extension is missed for source *FILENAME* COFF-file, then .OUT extension is assumed. The following is list of command line options for *TP6COFF.EXE* utility, which are grouped into several functional groups.

Upload Mode Control

-lr	Use *RESET* mode for uploading of COFF-file. COFF-file is uploaded while holding DSP in 'RESET' state. This mode is used to upload program/data into all DSP memory areas. DSP can be placed into the 'RUN' state on exit from *TP6COFF.EXE* utility using *-hcr0* command line option. The *-lr* option is assumed as default if *-ln* options is not specified.
-ln	Use *STANDARD* mode for uploading of COFF-file. This mode is used to upload run-time data into DPRAM area (*TORNADO-P62xx/P67* only) and into all DSP memory areas while on-board DSP is in the 'RUN' state.

-xi Exclude uploading of DSP on-chip memory/peripherals areas when using the *RESET* mode for uploading. This option must be used together with *-lr* option for *TORNADO-P62xx/P67* only.

Restarting DSP on Exit

-hcr0 Put DSP to the 'RUN' state on exit from *TP6COFF.EXE* utility.

Viewing Directory of COFF-file

-d List directory (sections loading information) for COFF-file. COFF-file will be not loaded into *TORNADO-P6x* environment an all other command line options specified will be ignored.

Board selection options

-i62hN (-i2hN) Select *TORNADO-P62* board with the PCI-bus index *#N* (*N* must be a decimal value within the 0..31 range).

-i67hN (-i7hN) Select *TORNADO-P67* board with the PCI-bus index *#N* (*N* must be a decimal value within the 0..31 range).

-i6202hN Select *TORNADO-P6202* board with the PCI-bus index *#N* (*N* must be a decimal value within the 0..31 range).

-i6203hN Select *TORNADO-P6203* board with the PCI-bus index *#N* (*N* must be a decimal value within the 0..31 range).

-i6414hN Select *TORNADO-P6414* board with the PCI-bus index *#N* (*N* must be a decimal value within the 0..31 range).

-i6415hN Select *TORNADO-P6415* board with the PCI-bus index *#N* (*N* must be a decimal value within the 0..31 range).

-i6416hN Select *TORNADO-P6416* board with the PCI-bus index *#N* (*N* must be a decimal value within the 0..31 range).

Utility options

-? Display list of available options for *TP6COFF.EXE* utility. Help list is also displayed when *TP6COFF.EXE* utility is invoked without command line options and parameters.

In case no errors are detected by *TP6COFF.EXE* utility, then exit code '0' will be returned, otherwise exit code '1' will be generated.

CAUTION

In case no board selection option is specified for *TP6COFF.EXE* software utility, then default *TORNADO-P6x* board will be selected as the following:
TORNADO-P62 board with index #0 will be selected as default in case it presents, otherwise *TORNADO-P67* board with index #0 will be selected as default in case it presents, otherwise *TORNADO-P6202* board with index #0 will be selected as default in case it presents, otherwise *TORNADO-P6203* board with index #0 will be selected as default in case it presents, otherwise *TORNADO-P6414* board with index #0 will be selected as default in case it presents, otherwise *TORNADO-P6415* board with index #0 will be selected as default in case it presents, otherwise *TORNADO-P6416* board with index #0 will be selected as default in case it presents.

CAUTION

SDRAM contents, which has been uploaded to the DSP SDRAM area using *TP6COFF.EXE* software utility, might be corrupted in case the *-hcr0* command line option (put DSP to the 'RUN' state) is not specified for *TP6COFF.EXE* software utility along with the uploaded filename.

CAUTION

If *TP6COFF.EXE* utility is used with *-lr* command line option and if either emulation controller *ECC* is active or external JTAG emulator is connected, then the following error message may appear:

error: missing DSP handshaking

This error message states that the TMS320C6x DSP cannot be initialized correctly during uploading of TMS320C6x DSP environment areas, which are not directly available from host PCI-bus interface. This problem is caused by DSP on-chip execution controller that is locked by attached emulator or *ECC/UECM*.

In order to avoid this problem you have to reset the *ECC* or external JTAG emulator. External JTAG emulator might be reset via supplied software reset utility, whereas *ECC* might be reset by invoking the *TP6CC.EXE* software utility program with the *-er* command line option.

Appendix A. Board Layout and Physical Dimensions

This Appendix includes a summarized description for the *TORNADO-P6x* on-board configuration jumpers, connectors, switches, sockets and LED indicators, and provides mechanical dimensions for *TORNADO-P6x* boards.

Layouts for on-board configuration jumpers, connectors, switches, sockets and LED indicators for the *TORNADO-P6x* DSP systems are presented at figures A-1a and A-1b.

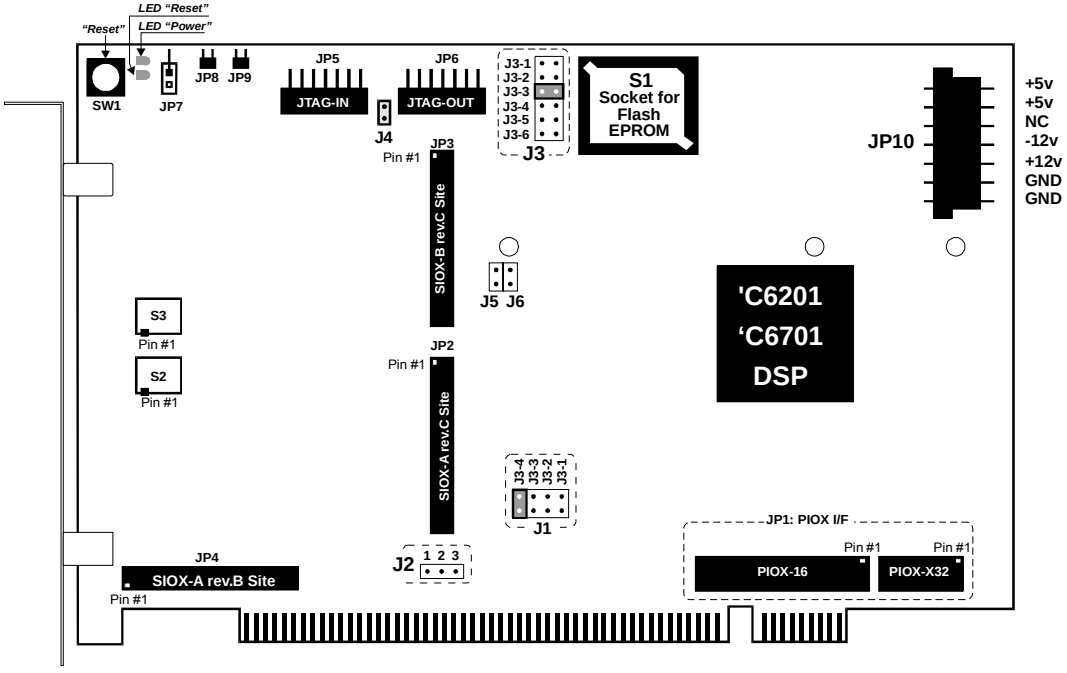


Fig.A-1a. On-board layout for *TORNADO-P62/P67* DSP systems.

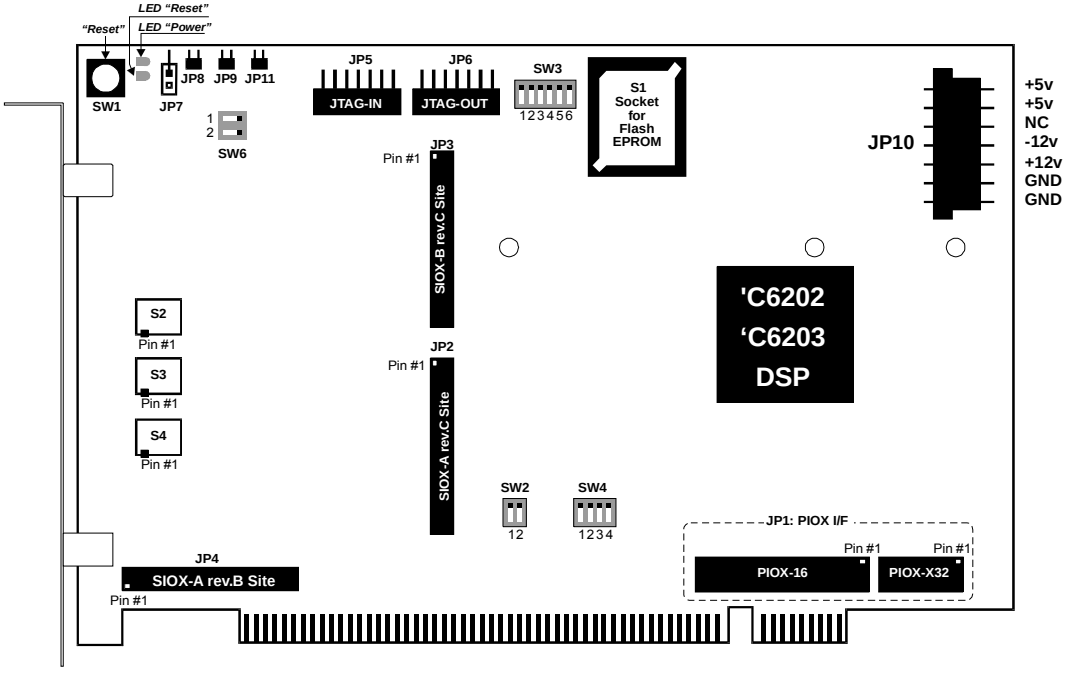


Fig.A-1b. On-board layout for *TORNADO-P6202/P6203* DSP systems.

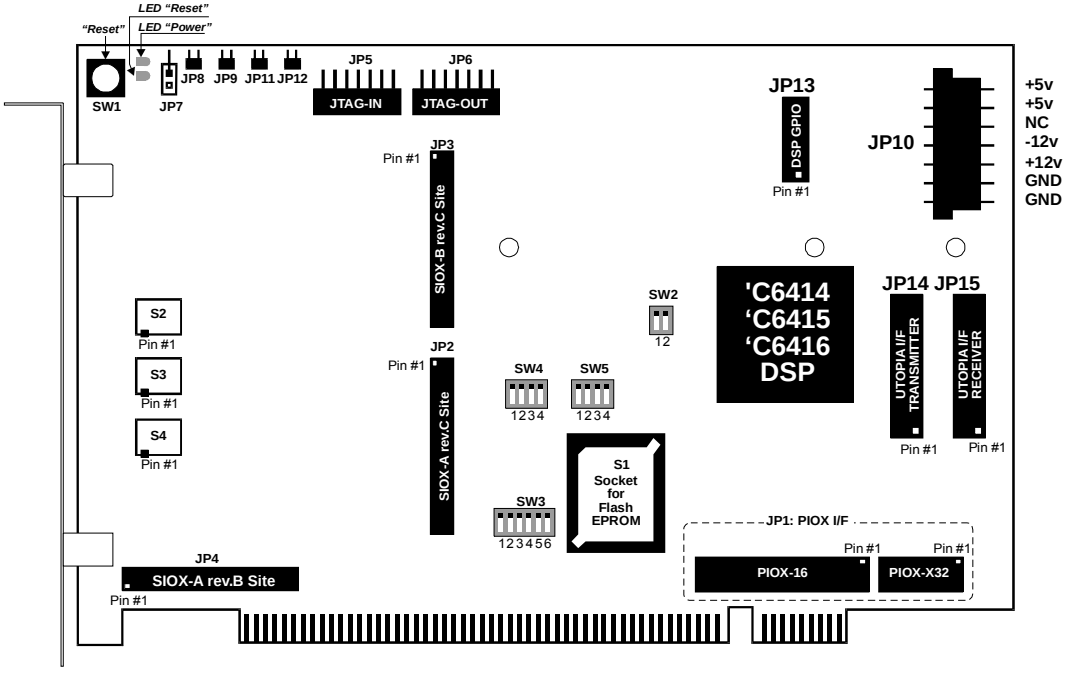


Fig.A-1c. On-board layout for *TORNADO-P64xx* DSP systems.

A.1 On-board Switches

On-board switches for *TORNADO-P6x* DSP systems are listed in table A-1.

Table A-1. On-board switches for *TORNADO-P6x*.

Switch ID	switch function description	reference information
SW1	Reset pushbutton for TMS320C6x DSP stand-alone operation mode.	Section 2.2.
SW2	TMS320C6x DSP bootmode configuration. (*TORNADO-P6202/P6203/P64xx* only)	Section 2.2, tables 2-2a and 2-2b
SW3	FLASH/EPROM type selector. (*TORNADO-P6202/P6203/P64xx* only)	Section 2.2 table 2-5

SW4-1	SIO-1 port configuration for SIOX-A rev.B/C sites. (*TORNADO-P6202/P6203/P64xx* only)	Section 2.5 tables 2-27 and 2-29
SW4-2	SIO ports configuration for SIOX-B rev.C site. (*TORNADO-P6202/P6203/P64xx* only)	Section 2.5 tables 2-28 and 2-30
SW4-3	TMS320C6x DSP timer-0 IN/OUT configuration. (*TORNADO-P6202/P6203* only)	Sections 2.2, 2.4, 2.5 figure 2-4b
SW4-3	TMS320C6415/C6416 DSP external interface selector (*TORNADO-P6415/P6416* only)	Sections 2.2, 2.5 table 2-14
SW4-4	TMS320C6x DSP timer-1 IN/OUT configuration. (*TORNADO-P6202/P6203* only)	Sections 2.2, 2.4, 2.5 figure 2-4b
SW4-4	JTAG path terminator. (*TORNADO-P64xx* only)	Section 2.6
SW5-1	TMS320C6x DSP timer-0 IN/OUT configuration. (*TORNADO-P64xx* only)	Sections 2.2, 2.4, 2.5 figure 2-4c
SW5-2	TMS320C6x DSP timer-1 IN/OUT configuration. (*TORNADO-P64xx* only)	Sections 2.2, 2.4, 2.5 figure 2-4c
SW5-3	TMS320C6x DSP timer-2 IN/OUT configuration. (*TORNADO-P64xx* only)	Sections 2.2, 2.4, 2.5 figure 2-4c
SW6-1	JTAG path terminator. (*TORNADO-P6202/P6203* only)	Section 2.6

A.2 On-board Jumpers

On-board configuration jumpers for *TORNADO-P6x* DSP systems are listed in table A-2.

Table A-2. On-board configuration jumpers for *TORNADO-P6x*.

jumper ID	jumper function description	reference information
J1	TMS320C6x DSP Bootmode configuration. (*TORNADO-P62/P67* only)	Section 2.2 table 2-2a
J2	SIOX-B rev.C site ports configuration ("direct" or "cross-wiring" selector). (*TORNADO-P62/P67* only)	Section 2.5 table 2-26
J3	FLASH/EPROM chip type selector. (*TORNADO-P62/P67* only)	Section 2.2 table 2-5.
J4	JTAG path terminator. (*TORNADO-P62/P67* only)	Section 2.6

J5	TMS320C6x DSP timer-0 IN/OUT mode for SIOX-A/B and PIOX/PIOX-16 sites. (*TORNADO-P62/P67* only)	Sections 2.2, 2.4, 2.5 figure 2-4a
J6	TMS320C6x DSP Timer-1 IN/OUT mode for SIOX-A/B and PIOX/PIOX-16 sites. (*TORNADO-P62/P67* only)	Sections 2.2, 2.4, 2.5 figure 2-4a

A.3 On-board Connectors

On-board connectors for *TORNADO-P6x* DSP systems are listed in table A-3.

Table A-3. On-board connectors for *TORNADO-P6x*.

connector ID	connector function description	reference information
JP1	PIOX/PIOX-16 DCM site interface connector.	Section 2.4 figure .2-25.
JP2 *JP3*	SIOX-A/B rev.C DCM site interface connectors.	Section 2.5 figure 2-17.
JP4	SIOX-A rev.B DCM site interface connector.	Section 2.5 figure 2-16
JP5 *JP6*	JTAG-IN and JTAG-OUT connectors.	Section 2.6
JP7	External reset connector for DSP stand-alone operation.	Section 2.2 figure 2-7
JP8	External clock (CLKS) connector for McBSP-0 of TMS320C6x DSP.	Section 2.5 figures 2-18a, 2-18b, 2-18c
JP9	External clock (CLKS) connector for McBSP-1 of TMS320C6x DSP.	Section 2.5 figures 2-18a, 2-18b, 2-18c
JP10	External power connector for stand-alone operation.	Section 2.2 figure 2-8
JP11	External clock (CLKS) connector for McBSP-2 of TMS320C6x DSP. (*TORNADO-P6202/P6203/P64xx* only)	Section 2.5 figures 2-18b, 2-18c
JP12	TMS320C64xx DSP on-chip timer-2 I/O connector. (*TORNADO-P64xx* only)	Section 2.2 figure 2-4c

JP13	TMS320C64xx DSP GPIO connector. (*TORNADO-P64xx* only)	Section 2.2 figure 2-6
JP14	UTOPIA interface transmitter connector. (*TORNADO-P64xx* only)	Section 2.2 figure 2-15b
JP15	UTOPIA interface receiver connector. (*TORNADO-P64xx* only)	Section 2.2 figure 2-15a

A.4 On-board Sockets

On-board sockets for *TORNADO-P6x* DSP systems are listed in table A-4.

Table A-4. On-board sockets for *TORNADO-P6x*.

socket ID	switch function description	reference information
S1	PLCC-32 socket for FLASH/EPROM (5v power supply).	Section 2.2, 3.2 figure 3-1.
S2	DIP-8 socket for TTL/CMOS 5v crystal oscillator for external clock source of McBSP-0 serial port of TMS320C6x DSP.	Section 2.5 figures 2-18a, 2-18b, 2-18c
S3	DIP-8 socket for TTL/CMOS 5v crystal oscillator for external clock source of McBSP-1 serial port of TMS320C6x DSP.	Section 2.5 figures 2-18a, 2-18b, 2-18c
S4	DIP-8 socket for TTL/CMOS 5v crystal oscillator for external clock source of McBSP-2 serial port of TMS320C6x DSP. (*TORNADO-P6202/P6203/P64xx* only)	Section 2.5 figures 2-18b, 2-18c

A.5 On-board LED Indicators

On-board LED indicators for *TORNADO-P6x* DSP systems are listed in table A-5.

Table A-5. On-board LED for *TORNADO-P6x*.

LED color	LED function description
GREEN	Power indicator.
RED	DSP reset indicator.

A.6 Physical dimensions for *TORNADO-P6x* boards

Physical dimensions for *TORNADO-P6x* DSP system boards including physical positions for all mounting holes and daughter-card site header is presented at fig.A-2. More details are available from MicroLAB Systems upon request.

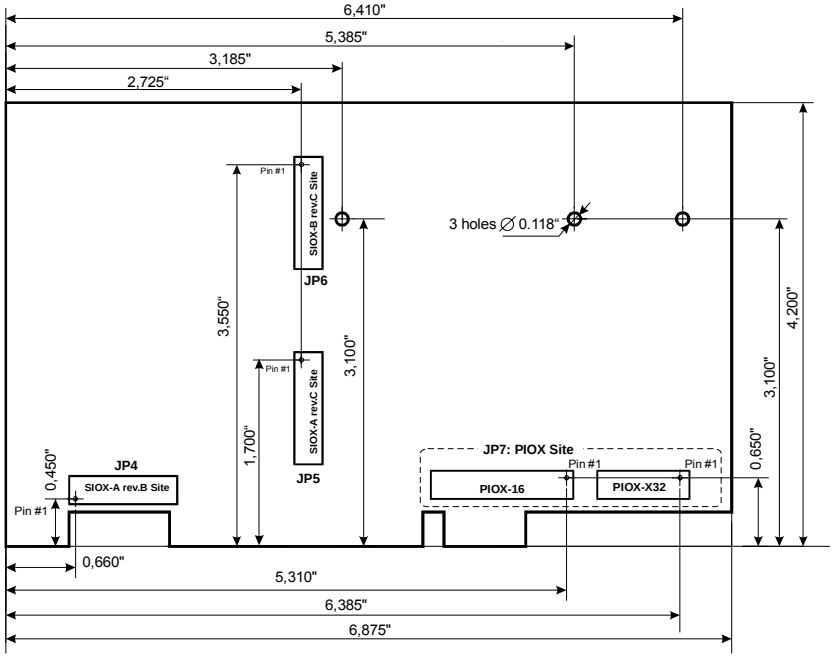


Fig.A-2. Physical dimensions for *TORNADO-P6x* DSP system boards.

Appendix B. AMCC S5933 PCI-Bus Controller

This Appendix contains architectural and programming details for AMCC S5933 (and S5935) PCI-bus controller (PCIC), which is used in host PCI-bus interface of *TORNADO-Pxxxx* PCI-bus plug-in DSP systems.

CAUTION

AMCC S5933 and S5935 PCIC appear as identical devices and differ in minor details about PCI-bus signal processing, which is not important for programming of *TORNADO-Pxxxx* applications. Therefore, the 'AMCC S5933 PCIC' notation will be used hereafter for all information applicable for both AMCC S5933 and S5935 PCIC.

CAUTION

TORNADO-Pxxxx notation denotes that provided information is applicable for all *TORNADO* DSP systems for PCI-bus.

Should provided information be *TORNADO* platform specific, then particular type of *TORNADO* DSP system (either *TORNADO-P33*, or *TORNADO-P62*, etc) will be highlighted.

It is highly recommended for *TORNADO-Pxxxx* users to read this Appendix before refer to original AMCC S5933 PCIC User's Guide, since AMCC S5933 PCIC specific information provided in this Appendix has been carefully linked to *TORNADO-Pxxxx* specific details (board architecture, register addressing, access modes, etc) and all minor details and unused AMCC S5933 PCIC resources have been omitted. In most cases information provided in this Appendix will be sufficient for design *TORNADO-Pxxxx* applications and it will be not required to refer to AMCC S5933 PCIC User's Guide.

CAUTION

This Appendix contains only those details about AMCC S5933 (S5935) PCIC, which are required for understanding of PCIC operation and for design of *TORNADO-Pxxxx* applications.

This Appendix does not contain other minor details (as timing diagrams, pinout, PCI-bus details, etc) about AMCC S5933 (S5935) PCIC, which are not required for user application programming.

For all details about AMCC S5933 and S5935 PCIC refer to original AMCC S5933 PCIC User's Guide, which is supplied either in the paper or electronic form along with this manual.

B.1 AMCC S5933 PCIC Architecture and Host PCI-bus Interface of *TORNADO-Pxxxx* DSP Systems

AMCC S5933 PCIC is the industry-standard programmable PCI-bus controller device, which meets PCI-bus rev.2.x specifications and is used for interfacing of PCI adapters to host PCI-bus.

TORNADO-Pxxxx PCI-bus plug-in DSP systems use AMCC S5933 PCIC as the part of host PCI-bus interface in order to interface on-board host interface hardware resources to host PCI-bus.

General description for AMCC S5933 PCIC

AMCC S5933 PCIC has been designed as the 'bridge' between host PCI-bus and on-board application specific local data bus.

Along with PCI-bus specific PCI configuration registers, AMCC S5933 PCIC also includes useful hardware resources for communication between host PCI-bus and on-board local bus, which typically contains CPU, via bidirectional FIFO and a set of bidirectional mailboxes. Also supported is the PCI-bus mastering feature, which can be used to transfer bidirectional data streams between host PCI-bus and on-board hardware under two-path AMCC S5933 PCIC DMA controller without utilization of host PC processing time.

AMCC S5933 PCIC has been selected as the 'heart' of host PCI-bus interface of *TORNADO-Pxxxx* PCI-bus plug-in DSP systems, since it well fits *TORNADO-Pxxxx* DSP systems architecture and provides all industry standard features and options for PCI-bus interfacing.

AMCC S5933 PCIC architecture and host PCI-bus interface of TORNADO-Pxxxx DSP systems

Figure B-1 presents simplified internal AMCC S5933 PCIC architecture and shows how AMCC S5933 PCIC is used in typical host PCI-bus interface of *TORNADO-Pxxxx* DSP systems.

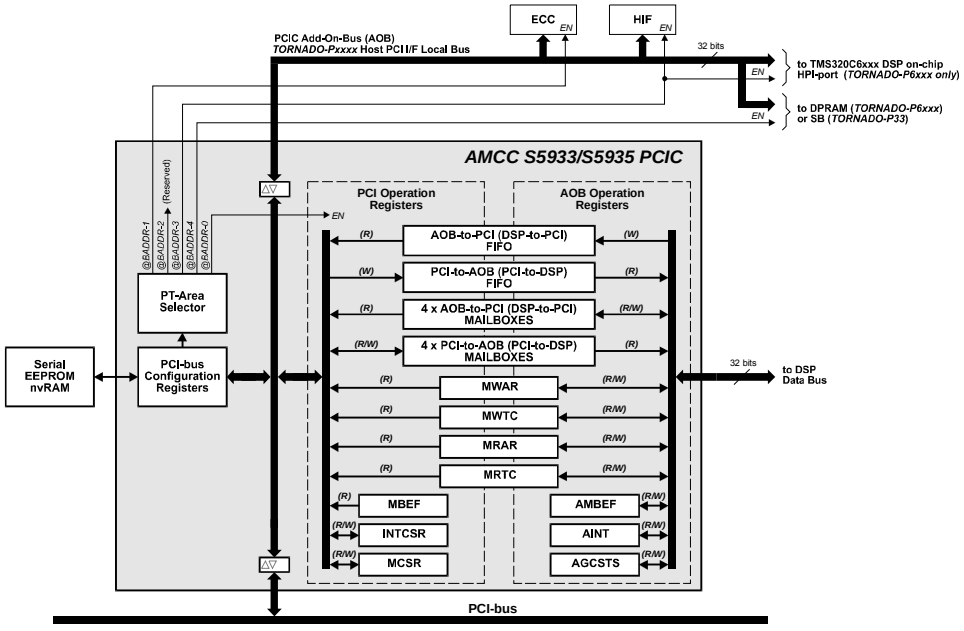


Fig. B-1. Host PCI-bus interface of *TORNADO-Pxxxx* PCI-bus plug-in DSP systems with AMCC S5933 PCIC.

AMCC S5933 PCIC performs transparent data forwarding between 32-bit host PCI-bus and 32-bit on-board local data bus of *TORNADO-Pxxxx* PCI-bus plug-in DSP system, which is also called as 'add-on bus' (AOB) in accordance with AMCC S5933 PCIC User's Guide.

On-board local data bus (AOB) of *TORNADO-Pxxxx* host PCI-bus interface typically comprises of the following on-board hardware areas (peripherals):

- host interface registers (HIF), which include on-board DSP control registers and DSP on-chip HPI port registers (*TORNADO-P6x* DSP systems only)
- either left port of on-board dual-port RAM (DPRAM) for *TORNADO-P6x* DSP systems or on-board shared bus (SB) access buffers for *TORNADO-P3x* DSP systems
- emulation controller chip (*ECC*), which is used as on-board JTAG emulation controller for on-board TMS320 DSP.

CAUTION

Refer to section "Host PCI-bus Interface" of Chapter 2 of User's Guide for your particular *TORNADO-Pxxxx* DSP system for more details about areas of host PCI-bus interface.

It is important to note, that data transfer between host PCI-bus and on-board AOB local bus of *TORNADO-Pxxxx* host PCI-bus interface can be initiated by host PCI-bus only when host PC application performs access to PCI-bus I/O or memory address space to the corresponding area of *TORNADO-Pxxxx* host PCI-bus interface.

This means that AOB bus is always a passive PCI-bus resource, which can be accessed by external PCI-bus master only.

CAUTION

All accesses from host PCI-bus to on-board AOB local bus areas of *TORNADO-Pxxxx* host PCI-bus interface are performed with extra PCI-bus wait states, since these accesses shall be confirmed by external data ready signals, which are generated by external peripherals.

AMCC S5933 PCIC internal architecture comprises of the set of *PCI operation registers* and *AOB operation registers*, which are not directly involved into data transfer between PCI-bus and on-board AOB local bus of *TORNADO-Pxxxx* host PCI-bus interface, but instead shall be optionally used by host PC application and *TORNADO-Pxxxx* on-board DSP application correspondingly in order to communicate bidirectional FIFO, a set of bidirectional mailboxes, and to configure DSP controlled PCI-bus mastering (direct data transfer between on-board DSP and host PCI-bus environment using two-path AMCC S5933 PCIC on-chip DMA controllers). AMCC S5933 PCIC on-chip *PCI operation registers* can be accessed from PCI-bus only from host PC application, whereas AMCC S5933 PCIC on-chip *AOB operation registers* can be accessed by *TORNADO-Pxxxx* on-board DSP only from DSP application.

CAUTION

Although 'AMCC S5933 PCIC on-chip *AOB operation registers*' notation uses 'AOB' as the part of the name in original AMCC S5933 PCIC User's Guide, these registers are not the part of on-board AOB local bus of *TORNADO-Pxxxx* host PCI-bus interface and can be accessed by *TORNADO-Pxxxx* on-board DSP only.

The corresponding subsections below and next sections in this Appendix will provide more architectural and programming details for AMCC S5933 PCIC.

Allocation of host PCI-bus interface areas of TORNADO-Pxxxx DSP systems

Each area of on-board local AOB bus of *TORNADO-Pxxxx* host PCI-bus interface is allocated to unique address sub-space of either PCI-bus memory space or PCI-bus I/O space.

Allocation information for each area of local AOB bus of *TORNADO-Pxxxx* host PCI-bus interface is stored in external on-board serial EEPROM/nvRAM and is processed by PCI BIOS of host PC during PC boot procedure.

Particular allocated memory or I/O base address for each area are loaded by PCI BIOS to BADDR0..4 AMCC S5933 PCIC on-chip PCI configuration registers as the following:

- BADDR0 base address register contains PCI allocated I/O base address for AMCC S5933 PCIC on-chip *PCI operation registers*
- BADDR1 base address register contains PCI allocated I/O base address for *ECC* area of *TORNADO-Pxxxx* host PCI-bus interface
- BADDR2 base address register is not used and is reserved fir future expansion

- BADDR3 base address register contains PCI allocated memory base address for DPRAM area for *TORNADO-P6x* host PCI-bus interface and for SB access area for *TORNADO-P3x* host PCI-bus interface
- BADDR4 base address register contains PCI allocated I/O base address for HIF/HPI area for *TORNADO-P6x* host PCI-bus interface and for HIF area for *TORNADO-P3x* host PCI-bus interface.

AMCC S5933 PCIC on-chip PCI operation registers

AMCC S5933 PCIC on-chip *PCI operation registers* are not directly involved into data transfer between PCI-bus and on-board AOB local bus of *TORNADO-Pxxxx* host PCI-bus interface, but instead shall be optionally used by host PC application in order to communicate with *TORNADO-Pxxxx* on-board DSP application via bidirectional FIFO and a set of bidirectional mailboxes, in order to configure host PCI-bus interrupt request source and to monitor status of DSP controlled PCI-bus mastering data transfers.

AMCC S5933 PCIC on-chip *PCI operation registers* of *TORNADO-Pxxxx* host PCI-bus interface are mapped into PCI-bus I/O address space using AMCC S5933 PCIC on-chip BADDR0 PCI configuration register and can be accessed from PCI-bus only.

AMCC S5933 PCIC on-chip *PCI operation registers* of *TORNADO-Pxxxx* host PCI-bus interface comprise of the following 32-bit registers:

- 8-level 32-bit bidirectional FIFO, which is on the other side is available for *TORNADO-Pxxxx* on-board DSP application via corresponding AMCC S5933 PCIC on-chip *AOB operation registers*. Note, that PCI-to-AOB FIFO register appears as write-only on the host PCI operation register side and as read-only on the DSP AOB operation register side. Instead, AOB-to-PCI FIFO register appears as read-only on the host PCI operation register side and as write-only on the DSP AOB operation register side.
- A set of four 32-bit PCI-to-AOB outgoing mailbox registers, which is on the other side are available for *TORNADO-Pxxxx* on-board DSP application via corresponding AMCC S5933 PCIC on-chip *AOB operation registers* as a set of four incoming mailbox registers. Note, that PCI-to-AOB mailbox registers appear as read/write on the host PCI operation register side and as read-only on the DSP AOB operation register side.
- A set of four 32-bit AOB-to-PCI incoming mailbox registers, which is on the other side are available for *TORNADO-Pxxxx* on-board DSP application via corresponding AMCC S5933 PCIC on-chip *AOB operation registers* as a set of four outgoing mailbox registers. Note, that AOB-to-PCI mailbox registers appear as read-only on the host PCI operation register side and as read/write on the DSP AOB operation register side.
- MWAR, MWTC, MRAR and MRTC read-only registers, which on the other side are available for read/write for *TORNADO-Pxxxx* on-board DSP application via corresponding AMCC S5933 PCIC on-chip *AOB operation registers*. These registers are used to configure and monitor status of DSP controlled DSP-to-PCI and PCI-to-DSP PCI-bus mastering data transfers using two-path AMCC S5933 PCIC on-chip DMA controllers.
- MBEF, INTCSR, and MCSR read/write registers, which are used to get and clear status of FIFO and mailbox registers, to configure host PCI-bus request and to control user access to on-board serial EEPROM/nvRAM memory for host PC application.

CAUTION

All accesses from host PCI-bus to AMCC S5933 PCIC on-chip *PCI operation registers* are performed without PCI-bus wait states, since these accesses are internal AMCC S5933 PCIC.

For more details about AMCC S5933 PCIC on-chip *PCI operation registers* refer to the corresponding section later in this Appendix.

AMCC S5933 PCIC on-chip AOB operation registers

AMCC S5933 PCIC on-chip *AOB operation registers* are mapped into *TORNADO-Pxxxx* on-board DSP memory space and shall be optionally used by DSP application in order to communicate with host PC application for *TORNADO-Pxxxx* DSP system via bidirectional FIFO and a set of bidirectional mailboxes, in order to configure PCI-to-DSP interrupt request via AMCC S5933 PCIC, and to configure and monitor status of DSP controlled PCI-bus mastering data transfers.

CAUTION

Although 'AMCC S5933 PCIC on-chip *AOB operation registers*' notation uses 'AOB' as the part of the name in original AMCC S5933 PCIC User's Guide, these registers are not the part of on-board AOB local bus of *TORNADO-Pxxxx* host PCI-bus interface and can be accessed by *TORNADO-Pxxxx* on-board DSP only.

CAUTION

Refer to section "TMS320xxxx DSP Environment" of Chapter 2 of User's Guide for your particular *TORNADO-Pxxxx* DSP system for more details about mapping of AMCC S5933 PCIC on-chip AOB operation registers into memory space of on-board DSP.

AMCC S5933 PCIC on-chip *AOB operation registers* can be accessed from on-board DSP application only and comprise of the following 32-bit registers:

- 8-level 32-bit bidirectional FIFO, which is on the other side is available for *TORNADO-Pxxxx* on-host PC application via corresponding AMCC S5933 PCIC on-chip *PCI operation registers*. Note, that PCI-to-AOB FIFO register appears as write-only on the host PCI operation register side and as read-only on the DSP AOB operation register side. Instead, AOB-to-PCI FIFO register appears as read-only on the host PCI operation register side and as write-only on the DSP AOB operation register side.
- A set of four 32-bit PCI-to-AOB incoming mailbox registers, which is on the other side are available for *TORNADO-Pxxxx* on-host PC application via corresponding AMCC S5933 PCIC on-chip *AOB operation registers* as a set of four outgoing mailbox registers. Note, that PCI-to-AOB mailbox registers appear as read/write on the host PCI operation register side and as read-only on the DSP AOB operation register side.

- A set of four 32-bit AOB-to-PCI outgoing mailbox registers, which is on the other side are available for *TORNADO-Pxxxx* on-host PC application via corresponding AMCC S5933 PCIC on-chip *AOB operation registers* as a set of four incoming mailbox registers. Note, that AOB-to-PCI mailbox registers appear as read-only on the host PCI operation register side and as read/write on the DSP AOB operation register side.
- MWAR, MWTC, MRAR and MRTC read/write registers, which on the other side are available for *TORNADO-Pxxxx* on-host PC application as read-only AMCC S5933 PCIC on-chip *AOB operation registers*. These registers are used to configure and monitor status of DSP controlled DSP-to-PCI and PCI-to-DSP PCI-bus mastering data transfers using two-path AMCC S5933 PCIC on-chip DMA controllers.
- AMBEF, AINT, and AGCSTS read/write registers, which are used to get and clear status of FIFO and mailbox registers, to configure PCI-to-DSP interrupt request via AMCC S5933 PCIC, and to control user access to on-board serial EEPROM/nvRAM memory from DSP application.

CAUTION

All accesses from on-board DSP to AMCC S5933 PCIC on-chip *AOB operation registers* are performed with extra DSP wait states, since these accesses shall be synchronized with PCI-bus clock and shall be confirmed by AMCC S5933 PCIC data ready signal..

For more details about AMCC S5933 PCIC on-chip *AOB operation registers* refer to the corresponding section later in this Appendix.

DSP controlled PCI-bus mastering via AMCC S5933 PCIC

All *TORNADO-Pxxxx* PCI-bus plug-in DSP systems support DSP controlled PCI-bus mastering data transfers between host PCI-bus and on-board DSP via AMCC S5933 PCIC on-chip bidirectional FIFO under the control of AMCC S5933 PCIC on-chip two-path DMA controllers.

DSP controlled PCI-bus mastering data transfers can be performed in both PCI-to-DSP and DSP-to-PCI direction, which can occur simultaneously.

For more details about DSP controlled PCI-bus mastering refer to the corresponding section later in this Appendix.

User access to TORNADO-Pxxxx on-board serial EEPROM/nvRAM

All *TORNADO-Pxxxx* PCI-bus plug-in DSP systems support access to the user area of on-board serial EEPROM/nvRAM from both host PC applications and DSP applications.

TORNADO-Pxxxx on-board serial EEPROM/nvRAM is generally used to store allocation information for each area of local AOB bus of *TORNADO-Pxxxx* host PCI-bus interface, however this area occupies only first 128 bytes of serial EEPROM/nvRAM, whereas remaining 1920 bytes inside serial EEPROM/nvRAM can be used to store user defined non-volatile data.

Access to on-board serial EEPROM/nvRAM can be programmed via AMCC S5933 PCIC on-chip MCSR PCI operation register on host PC side and via AMCC S5933 PCIC on-chip AGCSTS AOB operation register on DSP side.

CAUTION

Care shall be taken by host PC and DSP applications in order to exclude simultaneous access to on-board serial EEPROM/nvRAM and in order to avoid modification of PCI configuration block in serial EEPROM/nvRAM.

For more details about programming on-board serial EEPROM/nvRAM refer to the corresponding section later in this Appendix.

Access to AMCC S5933 PCIC when TORNADO-Pxxxx DSP system is used for stand-alone applications

All *TORNADO-Pxxxx* PCI-bus plug-in DSP systems support stand-lone operation mode from external power supply, i.e. when *TORNADO-Pxxxx* board is unplugged from host PCI-bus slot.

In case *TORNADO-Pxxxx* DSP system is unplugged from host PCI-bus slot and operates from external power, then on-board AMCC S5933 PCIC is disabled and access to AMCC S5933 PCIC on-chip *AOB operation registers* from DSP application is disabled.

B.2 AMCC S5933 PCIC on-chip PCI Operation Registers

This section provides details about AMCC S5933 PCIC on-chip *PCI operation registers*, which can be optionally used by host PC application to communicate with *TORNADO-Pxxxx* on-board DSP application via bidirectional FIFO and a set of bidirectional mailboxes, in order to configure host PCI-bus interrupt request source and to monitor status of DSP controlled PCI-bus mastering data transfers.

AMCC S5933 PCIC on-chip *PCI operation registers* are not directly involved into data transfer between PCI-bus and on-board AOB local bus of *TORNADO-Pxxxx* host PCI-bus interface (refer to fig.B-1).

AMCC S5933 PCIC on-chip PCI operation registers list and mapping

AMCC S5933 PCIC on-chip PCI operation registers of *TORNADO-Pxxxx* host PCI-bus interface are mapped as 16 consecutive 32-bit DWORD registers into PCI-bus I/O address space using AMCC S5933 PCIC on-chip BADDR0 PCI configuration register and can be accessed from PCI-bus only.

AMCC S5933 PCIC on-chip PCI operation registers are the primary method of communication between the PCI and DSP buses in *TORNADO-Pxxxx* DSP systems. Data, software-defined commands and command parameters can be either exchanged through the mailboxes, transferred through the FIFO in blocks under program control, or transferred using the FIFO under Bus Master control. Table B-1 lists the PCI Bus Operation Registers.

Table B-1. PCI Operation Registers.

Abbreviation used in AMCC S5933 PCIC User's Guide [4]	***Abbreviation used in TORNADO-Pxxxx User's Guide*** [3]	***PCI-bus I/O Address***	***Access mode***	***Value on PC reset***	***Description***
OMB1	*HOST_PCIC_OMBX0_RG*	BADDR0+00h	r/w	-	Outgoing Mailbox Register 1
OMB2	*HOST_PCIC_OMBX1_RG*	BADDR0+04h	r/w	-	Outgoing Mailbox Register 2
OMB3	*HOST_PCIC_OMBX2_RG*	BADDR0+08h	r/w	-	Outgoing Mailbox Register 3
OMB4	*HOST_PCIC_OMBX3_RG*	BADDR0+0Ch	r/w	-	Outgoing Mailbox Register 4
IMB1	*HOST_PCIC_IMBX0_RG*	BADDR0+10h	r	-	Incoming Mailbox Register 1
IMB2	*HOST_PCIC_IMBX1_RG*	BADDR0+14h	r	-	Incoming Mailbox Register 2
IMB3	*HOST_PCIC_IMBX2_RG*	BADDR0+18h	r	-	Incoming Mailbox Register 3
IMB4	*HOST_PCIC_IMBX3_RG*	BADDR0+1Ch	r	-	Incoming Mailbox Register 4
FIFO	*HOST_PCIC_FIFO_RG*	BADDR0+20h	r/w	-	FIFO Register port (bidirectional)
MWAR	*HOST_PCIC_MWAR_RG*	BADDR0+24h	r	00000000H	Master Write Address Register
MWTC	*HOST_PCIC_MWTC_RG*	BADDR0+28h	r	00000000H	Master Write Transfer Count Register
MRAR	*HOST_PCIC_MRAR_RG*	BADDR0+2Ch	r	00000000H	Master Read Address Register
MRTC	*HOST_PCIC_MRTC_RG*	BADDR0+30h	r	00000000H	Master Read Transfer Count Register
MBEF	*HOST_PCIC_MBEF_RG*	BADDR0+34h	r	00000000H	Mailbox Empty/Full Status
INTCSR	*HOST_PCIC_INTCSR_RG*	BADDR0+38h	r/w	00000000H	Interrupt Control/Status Register
MCSR	*HOST_PCIC_MCSR_RG*	BADDR0+3Ch	r/w	000000E6H	Bus Master Control/Status Register

Notes:
1. '*BADDR0'* denotes I/O base address of AMCC S5933 PCIC on-chip PCI operation registers area of host PCI-bus interface.
2. Register access modes: *r* - read only, *w* - write only, *r/w* - read/write.
3. This abbreviation is used in *TORNADO-Pxxxx* User's Guide in sections "TMS320xxxx DSP Environment" and "Host PCI-bus Interface" of Chapter 2.
4. This abbreviation is used in original AMCC S5933 PCIC User's Guide.

outgoing mailbox registers (OMB)

These four read/write DWORD registers provide a method for sending command or parameter data to the DSP environment. PCI bus operations to these registers may be in any width (byte, word, or DWORD).

Writing to these registers can be a source for DSP interrupt request (if desired) by enabling their interrupt generation through the use of the AOB interrupt control/status register.

incoming mailbox registers (IMB)

These four read-only DWORD registers provide a method for receiving user defined data from the DSP environment. PCI bus read operations to these registers may be in any width (byte, word, or DWORD). Only read operations are supported.

Reading from these registers can optionally cause an DSP interrupt request (if desired) by enabling their interrupt generation through the use of the Add-On's interrupt control/status register .

Mailbox 4 (*HOST_PCIC_IMBX3_RG*), byte 3 only exists when active DSP-to-PCI interrupt request is generated in accordance with the *HIF_IM_RG* and *HIF_IS_RG* HIF registers setting of *TORNADO-Pxxxx* host PCI-bus interface. Refer to section "Host PCI-bus Interface" of Chapter 2 of User's Guide for your *TORNADO-Pxxxx* DSP system for more details.

FIFO register port (FIFO)

This location provides access to the bidirectional FIFO. Separate registers are used when reading from or writing to the FIFO. Accordingly, it is not possible to read what was written to this location. The FIFO registers are implicitly involved in all bus master operations and, as such, should not be accessed during active bus master transfers.

When operating upon the FIFOs with software program transfers involving word or byte operations, the endian sequence of the FIFO should be established as outlined in figure B-8 and table B-3 of this Appendix, and in Section 11.1.1.2 of AMCC S5933 User's Guide in order to preserve the internal FIFO data ordering and flag management. The FIFO's fullness may be observed by reading the master control-status register, MCSR.

PCI controlled bus master write address register (MWAR)

This is the read-only register of *TORNADO-Pxxxx* host PCI-bus interface and is actually the mirror of the MWAR register from AMCC S5933 PCIC on-chip AOB operation register set, which is set by on-board DSP during DSP controlled PCI-bus mastering write data transfers.

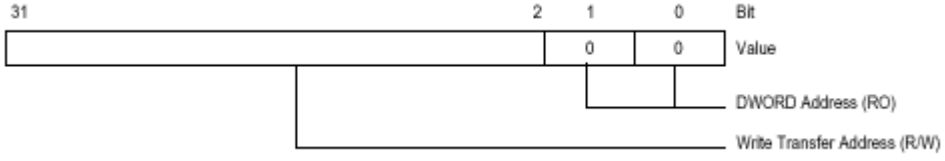


Fig. B-2. PCI Controlled Bus Master Write Address Register

It consists of a 30-bit counter with the low-order two bits hardwired as zeros. Transfers may be any non-zero byte length as defined by the transfer count register, MWTC, and must begin on a DWORD boundary. This DWORD boundary starting constraint is placed upon this controller's PCI bus master transfers so that byte lane alignment can be maintained between the S5933 controller's internal FIFO data path, the Add-On interface, and the PCI bus. Applications which require a non-DWORD starting boundary will need to move the first few bytes under software program control (and without using the FIFO) to establish a DWORD boundary. After the DWORD boundary is established the S5933 can begin the task of PCI bus master data transfers.

The Master Write Address Register is continually updated during the transfer process and will always be pointing to the next unwritten location. Reading of this register during a transfer process (done when the S5933 controller is functioning as a target, i.e. not a bus master) is permitted and may be used to monitor the progress of the transfer.

During the address phase for bus master write transfers, the two least significant bits presented on the PCI bus pins AD[31:0] will always be zero. This identifies to the target memory that the burst address sequence will be in a linear order rather than in an Intel 486 or Pentium™ cache line fill sequence. Also, the PCI bus address bit A1 will always be zero when this controller is the bus master. This signifies to the target that the S5933 controller is burst capable and that the target should not arbitrarily disconnect after the first data phase of this operation.

PCI controlled bus master write transfer count register (MWTC)

This is the read-only register of *TORNADO-Pxxxx* host PCI-bus interface and is actually the mirror of the MWTC register from AMCC S5933 PCIC on-chip AOB operation register set, which is set by on-board DSP during DSP controlled PCI-bus mastering write data transfers.

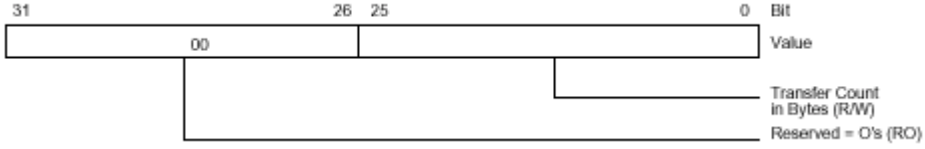


Fig. B-3. PCI Controlled Bus Master Write Transfer Count Register

The master write transfer count register is used to convey to the S5933 controller the actual number of bytes that are to be transferred. The value in this register is decremented with each bus master PCI write operation until the transfer count reaches zero. Upon reaching zero, the transfer operation ceases and an interrupt may be optionally generated to either the PCI or Add-On bus interface. Transfers which are not whole multiples of DWORDs in size result in a partial word ending cycle. This partial word ending cycle is possible since all bus master transfers for this controller are required to begin on a DWORD boundary.

PCI controlled bus master read address register (MRAR)

This is the read-only register of *TORNADO-Pxxxx* host PCI-bus interface and is actually the mirror of the MRAR register from AMCC S5933 PCIC on-chip AOB operation register set, which is set by on-board DSP during DSP controlled PCI-bus mastering read data transfers.

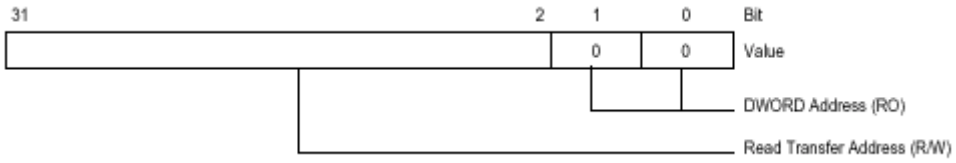


Fig. B-4. PCI Controlled Bus Master Read Address Register

This register is used to establish the PCI address for data moving to the Add-On bus from the PCI bus during PCI bus memory read operations. It consists of a 30-bit counter with the low-order two bits hardwired as zeros.

Transfers may be any non-zero byte length as defined by the transfer count register, MRTC and must begin on a DWORD boundary. This DWORD boundary starting constraint is placed upon this controller's PCI bus master transfers so that byte lane alignment can be maintained between the S5933 controller's internal FIFO data path, the Add-On interface and the PCI bus.

Applications which require a non-DWORD starting boundary will need to move the first few bytes under software program control (and without using the FIFO) to establish a DWORD boundary. After the DWORD boundary is established the S5933 can begin the task of PCI bus master data transfers.

The Master Read Address Register is continually updated during the transfer process and will always be pointing to the next unread location. Reading of this register during a transfer process (done when the S5933 controller is functioning as a target i.e., not a bus master) is permitted and may be used to monitor the progress of the transfer.

During the address phase for bus master read transfers, the two least significant bits presented on the PCI bus AD[31:0] will always be zero. This identifies to the target memory that the burst address sequence will be in a linear order rather than in an Intel 486 or Pentium™ cache line fill sequence. Also, the PCI bus address bit A1 will always be zero when this controller is the bus master. This signifies to the target that the controller is burst capable and that the target should not arbitrarily disconnect after the first data phase of this operation.

PCI controlled bus master read transfer count register (MRTC)

This is the read-only register of *TORNADO-Pxxxx* host PCI-bus interface and is actually the mirror of the MRAR register from AMCC S5933 PCIC on-chip AOB operation register set, which is set by on-board DSP during DSP controlled PCI-bus mastering read data transfers.

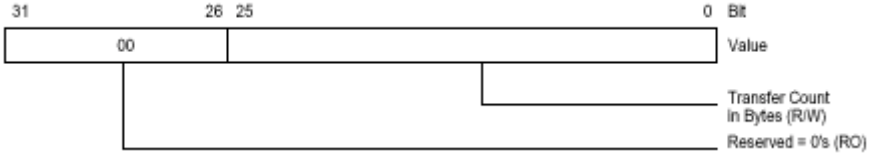


Fig. B-5. PCI Controlled Bus Master Read Transfer Count Register

The master read transfer count register is used to convey to the PCI controller the actual number of bytes that are to be transferred. The value in this register is decremented with each bus master PCI read operation until the transfer count reaches zero. Upon reaching zero, the transfer operation ceases and an interrupt may be optionally

generated to either the PCI or Add-On bus interface. Transfers which are not whole multiples of DWORDs in size result in a partial word ending cycle. This partial word ending cycle is possible since all bus master transfers for this controller are required to begin on a DWORD boundary.

mailbox empty full/status register (MBEF)

This register provides empty/full visibility of each byte within the mailboxes. The empty/full status for the Outgoing mailboxes is displayed on the low-order 16 bits and the empty/full status for the Incoming mail-boxes is presented on the high-order 16 bits.

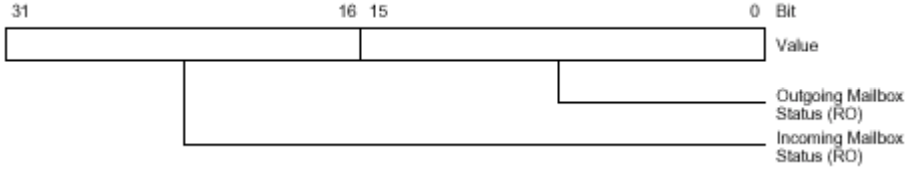


Fig. B-6. Mailbox Empty/Full Status Register

Table B-2. Mailbox Empty/Full Status Register

Bit	Description
31:16	Incoming Mailbox Status. This field indicates which incoming mailbox registers have been written by the Add-On interface but have not yet been read by the PCI bus. Each bit location corresponds to a specific byte within one of the four incoming mailboxes. A value of one for each bit signifies that the specified mailbox byte is full, and a value of zero signifies empty. The mapping of these status bits to bytes within each mailbox is as follows: Bit 31 = Incoming mailbox 4 byte 3 Bit 30 = Incoming mailbox 4 byte 2 Bit 29 = Incoming mailbox 4 byte 1 Bit 28 = Incoming mailbox 4 byte 0 Bit 27 = Incoming mailbox 3 byte 3 Bit 26 = Incoming mailbox 3 byte 2 Bit 25 = Incoming mailbox 3 byte 1 Bit 24 = Incoming mailbox 3 byte 0 Bit 23 = Incoming mailbox 2 byte 3 Bit 22 = Incoming mailbox 2 byte 2 Bit 21 = Incoming mailbox 2 byte 1 Bit 20 = Incoming mailbox 2 byte 0 Bit 19 = Incoming mailbox 1 byte 3 Bit 18 = Incoming mailbox 1 byte 2 Bit 17 = Incoming mailbox 1 byte 1 Bit 16 = Incoming mailbox 1 byte 0
15:00	Outgoing Mailbox Status. This field indicates which out going mail box registers have been written by the PCI bus interface but have not yet been read by the Add-On bus. Each bit location corresponds to a specific byte within one of the four outgoing mailboxes. A value of one for each bit signifies that the specified mailbox byte is full, and a value of zero signifies empty. The mapping of these status bits to bytes within each mailbox is as follows: Bit 15 = Outgoing mailbox 4 byte 3 Bit 14 = Outgoing mailbox 4 byte 2 Bit 13 = Outgoing mailbox 4 byte 1 Bit 12 = Outgoing mailbox 4 byte 0 Bit 11 = Outgoing mailbox 3 byte 3 Bit 10 = Outgoing mailbox 3 byte 2 Bit 09 = Outgoing mailbox 3 byte 1 Bit 08 = Outgoing mailbox 3 byte 0 Bit 07 = Outgoing mailbox 2 byte 3 Bit 06 = Outgoing mailbox 2 byte 2 Bit 05 = Outgoing mailbox 2 byte 1 Bit 04 = Outgoing Mailbox 2 byte 0 Bit 03 = Outgoing Mailbox 1 byte 3 Bit 02 = Outgoing Mailbox 1 byte 2 Bit 01 = Outgoing Mailbox 1 byte 1 Bit 00 = Outgoing Mailbox 1 byte 0

A value of 1 signifies that a given mailbox has been written by one bus interface but has not yet been read by the corresponding destination interface. A PCI bus in-coming mailbox is defined as one in which data travels from the DSP environment into the PCI bus, and an outgoing mailbox is defined as one where data travels out from the PCI bus to DSP environment.

interrupt control/status register (INTCSR)

This register provides the method for choosing which conditions are to produce an interrupt request on the PCI bus interface, a method for viewing the cause of the interrupt, and a method for acknowledging (removing) the interrupt's assertion.

Available PCI-bus interrupt request sources are as the following:

- write transfer terminal count is zero

- read transfer terminal count is zero
- one of the outgoing mailboxes (1,2,3 or 4) becomes empty
- one of the incoming mailboxes (1,2,3 or 4) becomes full
- target abort
- master abort.

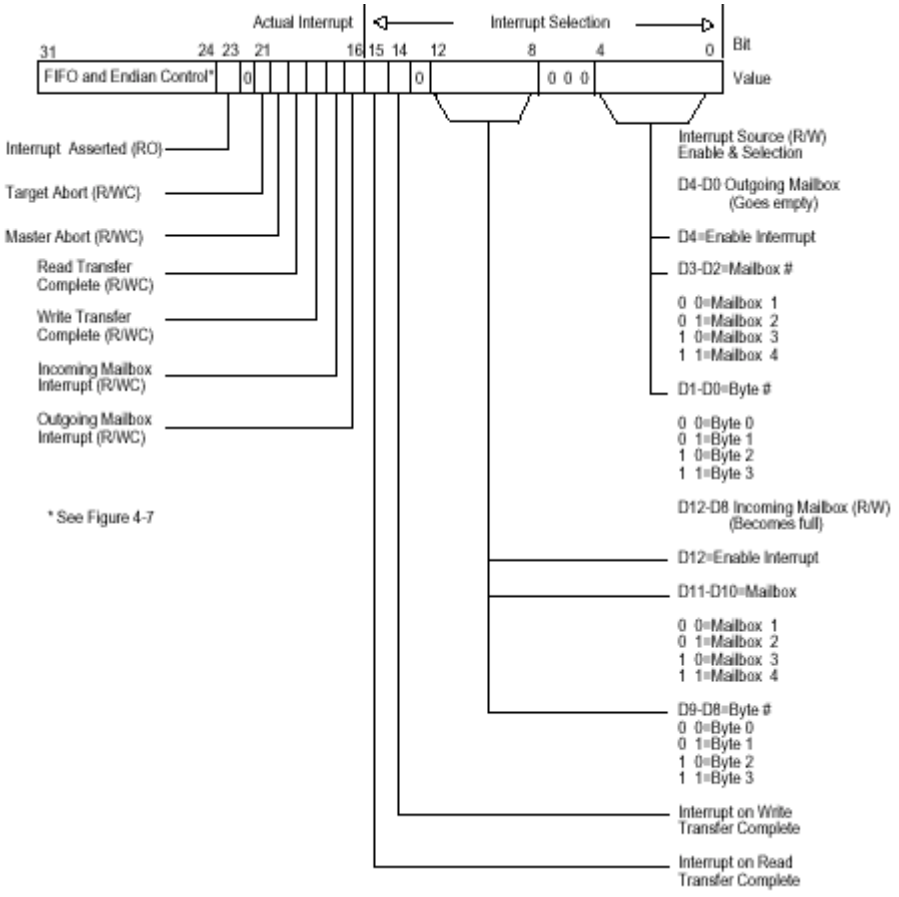


Fig. B-7. Interrupt Control/Status Register

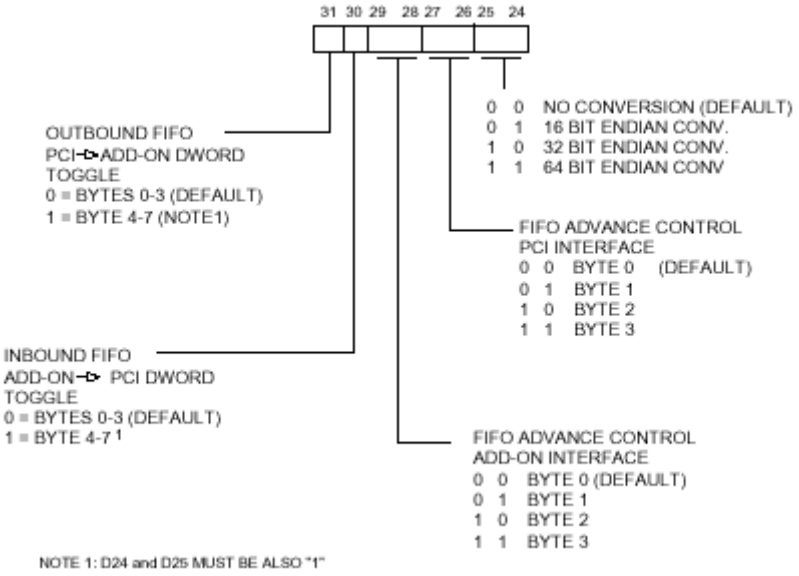


Fig. B-8. FIFO Management and Endian Control Byte

Table B-3. Interrupt Control/Status Register

Bit	***Description***
31:24	FIFO and Endian Control (section 11.1 of AMCC S5933 PCIC user's Guide).
23	Interrupt asserted. This read only status bit indicates that one or more of the four possible interrupt conditions is present. This bit is nothing more than the ORing of the interrupt conditions described by bits 19 through 16 of this register.
22	Reserved. Always zero.
21	Target Abort. This bit signifies that an interrupt has been generated due to the S5933 encountering a target abort during a PCI bus cycle while the S5933 was the current bus master. This bit operates as read or write one clear. A write to this bit with the data of "one" will cause this bit to be reset, a write to this bit with the data of "zero" will not change the state of this bit.
20	Master Abort. This bit signifies that an interrupt has been generated due to the S5933 encountering a Master Abort on the PCI bus. A master abort occurs when there is no target response to a PCI bus cycle. This bit operates as read or write one clear. A write to this bit with the data of "one" will cause this bit be reset, a write to this bit with the data of "zero" will not change the state of this bit.
19	Read Transfer Complete. This bit signifies that an interrupt has been generated due to the completion of a PCI bus master operation involving the transfer of data from the PCI bus to DSP environment. This interrupt will occur when the Master Read Transfer Count register reaches zero. This bit operates as read or write one clear. A write to this bit with the data of "one" will cause this bit to be reset; a write to this bit with the data of "zero" will not change the state of this bit.

18	Write Transfer Complete. This bit signifies that an interrupt has been generated due to the completion of a PCI bus master operation involving the transfer of data to the PCI bus from DSP environment. This interrupt will occur when the Master Write Transfer Count register reaches zero. This bit operates as read or write one clear. A write to this bit with the data of "one" will cause this bit to be reset; a write to this bit with the data of "zero" will not change the state of this bit.
17	Incoming Mailbox Interrupt. This bit is set when the mailbox selected by bits 12 through 8 of this register are written by DSP. This bit operates as read or write one clear. A write to this bit with the data of "one" will cause this bit to be reset; a write to this bit with the data as "zero" will not change the state of this bit.
16	Outgoing Mailbox Interrupt. This bit is set when the mailbox selected by bits 4 through 0 of this register is read by DSP. This bit operates as read or write one clear. A write to this bit with the data of "one" will cause this bit to be reset; a write to this bit with the data of "zero" will not change the state of this bit.
15	Interrupt on Read Transfer Complete. This bit enables the occurrence of an interrupt when the read transfer count reaches zero. This bit is read/write.
14	Interrupt on Write Transfer Complete. This bit enables the occurrence of an interrupt when the write transfer count reaches zero. This bit is read/write.
13	Reserved. Always zero.
12	Enable incoming mailbox interrupt. This bit allows a write from the incoming mailbox register identified by bits 11 through 8 to produce a PCI interface interrupt. This bit is read/write.
11:10	Incoming Mailbox Interrupt Select. This field selects which of the four incoming mailboxes is to be the source for causing an incoming mailbox interrupt. This field is read/write.
9:8	Incoming Mailbox Byte Interrupt select. This field selects which byte of the mailbox selected by bits 10 and 11 above is to actually cause the interrupt. This field is read/write.
7:5	Reserved, Always zero.
4	Enable outgoing mailbox interrupt. This bit allows a read by DSP of the outgoing mailbox register identified by bits 3 through 0 to produce a PCI interface interrupt. This bit is read/write.
3:2	Outgoing Mailbox Interrupt Select. This field selects which of the four outgoing mailboxes is to be the source for causing an outgoing mailbox interrupt. This field is read/write.
1:0	Outgoing Mailbox Byte Interrupt select. This field selects which byte of the mailbox selected by bits 3 and 2 above is to actually cause the interrupt. This field is read/write.

master control/status register (MCSR)

This register provides for overall control of AMCC S5933 PCIC device, i.e. for software resets, FIFO status flags monitoring and for user access to serial EEPROM/nvRAM.

Generally, this register is also used to enable bus mastering for both data directions, but since *TORNADO-P6xxxx* DSP systems are configured for DSP controlled PCI-bus mastering ('AOB initiated PCI-bus mastering' in terms of AMCC S5933 PCIC User's Guide), then this register is not used for PCI-bus mastering control.

The following PCI bus controls are available:

- write priority over read
- read priority over write
- write transfer enable (this bit is not used in *TORNADO-Pxxxx* DSP systems)
- write master requests on 4 or more FIFO words available (full)
- read transfer enable (this bit is not used in *TORNADO-Pxxxx* DSP systems)
- read master requests on 4 or more FIFO available (empty)
- assert reset to Add-On (this bit is not used in *TORNADO-Pxxxx* DSP systems)
- reset Add-On to PCI (DSP-to-PCI) FIFO flags
- reset PCI to Add-On (PCI-to-DSP) FIFO flags
- reset mailbox empty full status flags
- write external non-volatile memory

The following PCI interface status flags are provided:

- PCI to Add-On (PCI-to-DSP) FIFO full
- PCI to Add-On (PCI-to-DSP) FIFO has four or more empty locations
- PCI to Add-On (PCI-to-DSP) FIFO empty
- Add-On to PCI (DSP-to-PCI) FIFO full
- Add-On to PCI (DSP-to-PCI) FIFO has four or more words loaded
- Add-On to PCI (DSP-to-PCI) FIFO empty
- PCI to Add-On transfer count is zero (this bit is not used in *TORNADO-Pxxxx* DSP systems)
- Add-On to PCI transfer count is zero (this bit is not used in *TORNADO-Pxxxx* DSP systems).

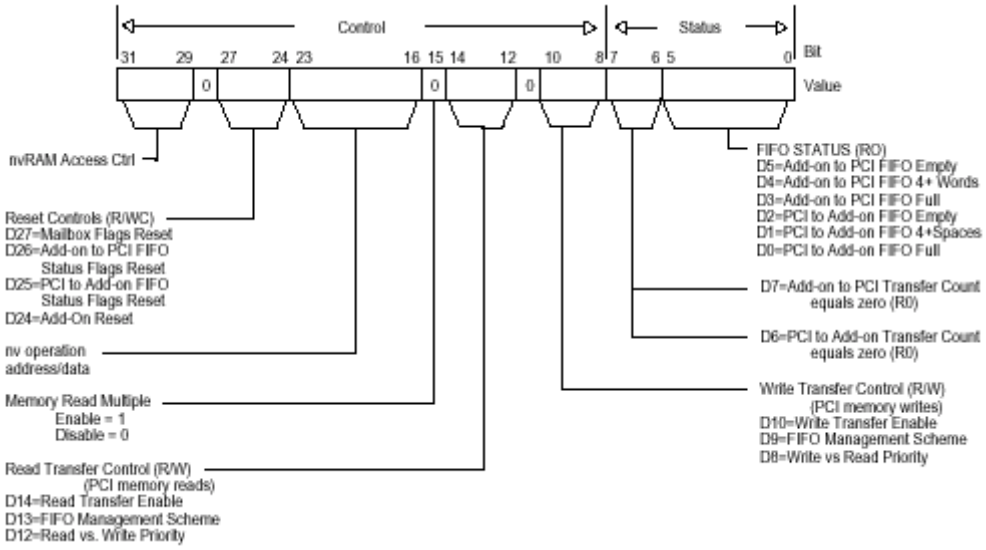


Fig. B-9. Bus Master Control/Status Register

Table B-4. Bus Master Control/Status Register

Bit	***Description***
31:29	nvRAM Access Control. This field provides a method for access to the optional external non-volatile memory. Write operations are achieved by a sequence of byte operations involving these bits and the 8-bit field of bits 23 through 16. The sequence requires that the low-order address, high order address, and then a data byte are loaded in order. Bit 31 of this field acts as a combined enable and ready for the access to the external memory. D31 must be written to a 1 before an access can begin, and subsequent accesses must wait for bit D31 to become zero (ready). *D31* *D30* *D29* *W/R* *nvRAM function* 0 X X W Inactive 1 0 0 W Load low address byte 1 0 1 W Load high address byte 1 1 0 W Begin write 1 1 1 W Begin read 0 X X R Ready 1 X X R Busy Cautionary note: The nonvolatile memory interface is also available for access by DSP (Add-On interface). Accesses by both DSP and PCI bus to the nvRAM are not directly supported by the S5933 device. Software must be designed to prevent the simultaneous access of nvRAM to prevent data corruption within the memory and provide for accurate data retrieval.
28	FIFO loop back mode.
27	Mailbox Flag Reset. Writing a one to this bit causes all mailbox status flags to become reset (EMPTY). It is not necessary to write this bit as zero because it is used internally to produce a reset pulse. Since reading of this bit will always produce zeros, this bit is write only.
26	DSP-to-PCI FIFO Status Reset. Writing a one to this bit causes the DSP-to-PCI (Bus master memory writes) FIFO empty flag to set indicating empty and the FIFO FULL flag to reset and the FIFO Four Plus word flag to reset. It is not necessary to write this bit as zero because it is used internally to produce a reset pulse. Since reading of this bit will always produce zeros, this bit is write only.
25	PCI-to-DSP FIFO Status Reset. Writing a one to this bit causes the PCI-to-DSP (Bus master memory reads) FIFO empty flag to set indicating empty and the FIFO FULL flag to reset and the FIFO Four Plus words available flag to set. It is not necessary to write this bit as zero because it is used internally to produce a reset pulse. Since reading of this bit will always produce zeros, this bit is write only.
24	This bit is not used in *TORNADO-Pxxxx* DSP systems.
23:16	Non-volatile memory address/data port. This 8-bit field is used in conjunction with bit 31, 30 and 29 of this register to access the external non-volatile memory. The contents written are either low address, high address, or data as defined by bits 30 and 29. This register will contain the external non-volatile memory data when the proper read sequence for bits 31 through 29 is performed.
15	This bit is not used in *TORNADO-Pxxxx* DSP systems.
14	This bit is not used in *TORNADO-Pxxxx* DSP systems.
13	Read FIFO management scheme. When set to a 1, this bit causes the controller to refrain from requesting the PCI bus unless it has four or more vacant FIFO locations to fill. Once the controller is granted the PCI bus or is in possession of the bus due to the write channel, this constraint is not meaningful. When this bit is zero the controller will request the PCI bus if it has at least one vacant FIFO

	word.
12	Read versus Write priority. This bit controls the priority of read transfers over write transfers. When set to a 1 with bit D8 as zero this indicates that read transfers always have priority over write transfers; when set to a one with D8 as one, this indicates that transfer priorities will alternate equally between read and writes.
11	Reserved. Always zero.
10	This bit is not used in *TORNADO-Pxxxx* DSP systems.
9	Write FIFO management scheme. When set to a one this bit causes the controller to refrain from requesting the PCI bus unless it has four or more FIFO locations filled. Once the S5933 controller is granted the PCI bus or is in possession of the bus due to the write channel, this constraint is not meaningful. When this bit is zero the controller will request the PCI bus if it has at least one valid FIFO word.
8	Write versus Read priority. This bit controls the priority of write transfers over read transfers. When set to a one with bit D12 as zero this indicates that write transfers always have priority over read transfers; when set to a one with D12 as one, this indicates that transfer priorities will alternate equally between writes and reads.
7	Add-On to PCI Transfer Count Equal Zero (RO). This bit is a one to signify that the write transfer count is all zeros.
6	PCI to Add-On Transfer Count Equals Zero (RO). This bit is a one to signify that the read transfer count is all zeros.
5	DSP-to-PCI FIFO Empty. This bit is a one when the DSP-to-PCI bus FIFO is completely empty.
4	DSP-to-PCI 4+ words. This bit is a one when there are four or more FIFO words valid within the DSP-to-PCI bus FIFO.
3	DSP-to-PCI FIFO Full. This bit is a one when the DSP-to-PCI bus FIFO is completely full.
2	PCI-to-DSP FIFO Empty. This bit is a one when the PCI-to-DSP FIFO is completely empty.
1	PCI-to-DSP FIFO 4+ spaces. This bit signifies that there are at least four empty words within the PCI-to-DSP FIFO.
0	PCI-to-DSP FIFO Full. This bit is a one when the PCI-to-DSP FIFO is completely full.

B.3 AMCC S5933 PCIC on-chip AOB Operation Registers

This section provides details about AMCC S5933 PCIC on-chip *AOB operation registers*, which comprise of 16 32-bit DWORDs (64 bytes) of data, control and status information, and are directly mapped into *TORNADO-Pxxxx* on-board DSP memory space.

AMCC S5933 PCIC on-chip AOB operation registers cab be optionally used by DSP application in order to communicate with host PC application for *TORNADO-Pxxxx* DSP system via bidirectional FIFO and a set of bidirectional mailboxes, in order to configure PCI-to-DSP interrupt request via AMCC S5933 PCIC, and to configure and monitor status of DSP controlled PCI-bus mastering data transfers.

AMCC S5933 PCIC on-chip AOB operation registers are available for *TORNADO-Pxxxx* on-board DSP only in case *TORNADO-Pxxxx* board is installed into PCI-bus slot of host PC.

This register group represents the primary method for communication between *TORNADO-Pxxxx* on-board DSP and PCI buses as viewed by the DSP. The flexibility of this arrangement allows a number of user-defined software protocols to be built. For example, data, software as-signed commands, and command parameters can be exchanged between the PCI and DSP buses using either the mailboxes or FIFOs with or without handshaking interrupts. The register structure is very similar to that of the AMCC S5933 PCIC on-chip PCI operation register set.

AOB operation registers list and DSP address mapping

Table B-5 lists the AMCC S5933 PCIC on-chip AOB operation register set available for access from *TORNADO-Pxxxx* on-board DSP.

Table B-5. AOB Operation Registers.

Abbreviation used in AMCC S5933 PCIC User's Guide [3]	*Abbreviation used in TORNADO-Pxxxx User's Guide* [2]	*DSP address for TORNADO-P3x DSP systems*	*DSP address for TORNADO-P6x DSP systems*	*Access mode*	*Value on PC reset*	*Description*
AFIFO	*DSP_PCIC_FIFO_RG*	900000h	000C0000h	r/w	-	Add-On (DSP) FIFO port
AMBEF	*DSP_PCIC_AMBEF_RG*	900001h	000C0004h	r	00000000H	Add-On (DSP) Mailbox Empty/Full Status
AINT	*DSP_PCIC_AINT_RG*	900002h	000C0008h	r/w	00000000H	Add-On (DSP) Interrupt control
AGCSTS	*DSP_PCIC_AGCSTS_RG*	900003h	000C000Ch	r/w	000000F4H	Add-On (DSP) General Control and Status Register
MWAR	*DSP_PCIC_MWAR_RG*	900004h	000C0010h	r/w	00000000H	Bus Master Write Address Register
MWTC	*DSP_PCIC_MWTC_RG*	900005h	000C0014h	r/w	00000000H	Bus Master Write Transfer Count
MRAR	*DSP_PCIC_MRAR_RG*	900006h	000C0018h	r/w	00000000H	Bus Master Read Address Register
MRTC	*DSP_PCIC_MRTC_RG*	900007h	000C001Ch	r/w	00000000H	Bus Master Read Transfer Count

AIMB1	*DSP_PCIC_IMBX0_RG*	900008h	000C0020h	r	-	Add-On (DSP) Incoming Mailbox Register #1
AIMB2	*DSP_PCIC_IMBX1_RG*	900009h	000C0024h	r	-	Add-On (DSP) Incoming Mailbox Register #2
AIMB3	*DSP_PCIC_IMBX2_RG*	90000Ah	000C0028h	r	-	Add-On (DSP) Incoming Mailbox Register #3
AIMB4	*DSP_PCIC_IMBX3_RG*	90000Bh	000C002Ch	r	-	Add-On (DSP) Incoming Mailbox Register #4
AOMB1	*DSP_PCIC_OMBX0_RG*	90000Ch	000C0030h	r/w	-	Add-On Outgoing Mailbox Register #1
AOMB2	*DSP_PCIC_OMBX1_RG*	90000Dh	000C0034h	r/w	-	Add-On (DSP) Outgoing Mailbox Register #2
AOMB3	*DSP_PCIC_OMBX2_RG*	90000Eh	000C0038h	r/w	-	Add-On (DSP) Outgoing Mailbox Register #3
AOMB4	*DSP_PCIC_OMBX3_RG*	90000Fh	000C003Ch	r/w	-	Add-On (DSP) Outgoing Mailbox Register #4

Notes:
1. Register access modes: *r* - read only, *w* - write only, *r/w* - read/write.
2. This abbreviation is used in *TORNADO-Pxxxx* User's Guide in sections "TMS320xxxx DSP Environment" and "Host PCI-bus Interface" of Chapter 2.
3. This abbreviation is used in original AMCC S5933 PCIC User's Guide.

CAUTION

Access to all AMCC S5933 PCIC on-chip AOB operation registers from *TORNADO-P3x* on-board DSP is performed using 32-bit data access cycles only.

Access to AMCC S5933 PCIC on-chip AOB operation registers (except for AFIFO register) from *TORNADO-P6x* on-board DSP can be performed using either of 8-/16-/32-bit data access cycles.

Access to AFIFO AMCC S5933 PCIC on-chip AOB operation register from *TORNADO-P6x* on-board DSP must be performed using 32-bit data access cycles only.

Add-on (DSP) incoming mailbox registers (AIMBx)

These four DWORD registers provide a method for receiving data, commands, or command parameters from the PCI interface.

These registers are read-only. Writes to this address space have no effect. Reading from one of these registers can optionally cause a PCI bus interrupt (if desired) when the PCI interrupt control/status register is properly configured (refer to section B.2).

Add-on (DSP) outgoing mailbox registers (AOMBx)

These four DWORD registers provide a method for sending data, commands, or command parameters or status to the PCI interface.

These registers may also be read. Writing to one of these registers can optionally cause a PCI bus interrupt (if desired) when the PCI interrupt control/status register is properly configured (refer to section B.2).

Mailbox 4 (*DSP_PCIC_OMBX3_RG*), byte 3 only exists when active DSP-to-PCI interrupt request is generated in accordance with the *HIF_IM_RG* and *HIF_IS_RG* HIF registers setting of *TORNADO-Pxxxx* host PCI-bus interface. Refer to section "Host PCI-bus Interface" of Chapter 2 of User's Guide for your *TORNADO-Pxxxx* DSP system for more details.

Add-on (DSP) FIFO register port (AFIFO)

This location provides access to the bidirectional FIFO. Separate registers are involved when reading and writing to this location. Accordingly, it is not possible to read what was written to this location.

The sequence of filling and emptying this FIFO is established by the PCI interface interrupt control and Status Register. The FIFO's fullness may be observed by reading the master control/status register, AGCSTS, described in section B.2.

CAUTION

Access to all AMCC S5933 PCIC on-chip AOB operation registers from *TORNADO-P3x* on-board DSP is performed using 32-bit data access cycles only.

Access to AFIFO AMCC S5933 PCIC on-chip AOB operation register from *TORNADO-P6x* on-board DSP must be performed using 32-bit data access cycles only.

DSP controlled bus master write address register (MWAR)

This register is used to establish the PCI address for data moving from the DSP environment to the PCI bus during PCI bus memory write operations. *TORNADO-Pxxxx* on-board DSP can read/write to this register, since *TORNADO-Pxxxx* DSP systems are configured to use DSP controlled (Add-On initiated) PCI-bus mastering.

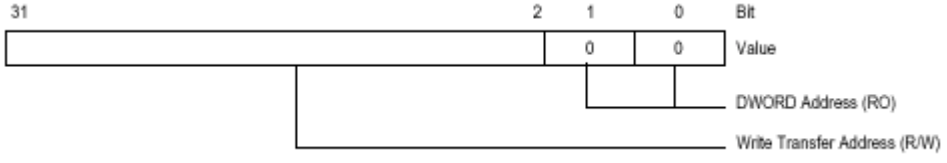


Fig. B-10. Add-On Controlled Bus Master Write Address Register

It consists of a 30-bit counter with the low-order two bits hardwired as zeros. Transfers may be any non-zero byte length as defined by the transfer count register, MWTC (refer to the corresponding subsection below), and

must begin on a DWORD boundary. This DWORD boundary starting constraint is placed upon this controller's PCI bus master transfers so that byte lane alignment can be maintained between the S5933 controller's internal FIFO data path, DSP, and the PCI bus.

Applications which require a non-DWORD starting boundary will need to move the first few bytes under software program control (and without using the FIFO) to establish a DWORD boundary. After the DWORD boundary is established the S5933 can begin the task of PCI bus master data transfers.

The Master Write Address Register is continually updated during the transfer process and will always be pointing to the next unwritten location. Reading of this register during a transfer process (done when the S5933 controller is functioning as a target, i.e. not a bus master) is permitted and may be used to monitor the progress of the transfer.

During the address phase for bus master write transfers, the two least significant bits presented on the PCI bus pins AD[31:0] will always be zero. This identifies to the target memory that the burst address sequence will be in a linear order rather than in an Intel 486 or Pentium™ cache line fill sequence. Also, the PCI bus address bit A1 will always be zero when this controller is the bus master. This signifies to the target that the S5933 controller is burst capable and that the target should not arbitrarily disconnect after the first data phase of this operation.

DSP controlled bus master read address register (MRAR)

This register is used to establish the PCI address for data moving to the DSP environment from the PCI bus during PCI bus memory read operations. *TORNADO-Pxxxx* on-board DSP can read/write to this register, since *TORNADO-Pxxxx* DSP systems are configured to use DSP controlled (Add-On initiated) PCI-bus mastering.

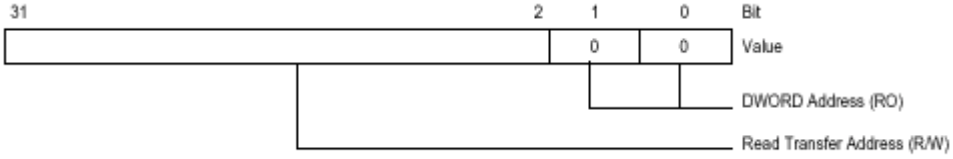


Fig. B-11. Add-On Controlled Bus Master Read Address Register

It consists of a 30-bit counter with the low-order two bits hardwired as zeros. Transfers may be any non-zero byte length as defined by the transfer count register, MRTC (refer to section B.2) and must begin on a DWORD boundary. This DWORD boundary starting constraint is placed upon this controller's PCI bus master transfers so that byte lane alignment can be maintained between the S5933 controller's internal FIFO data path, DSP, and the PCI bus.

Applications which require a non-DWORD starting boundary will need to move the first few bytes under software program control (and without using the FIFO) to establish a DWORD boundary. After the DWORD boundary is established the S5933 can begin the task of PCI bus master data transfers.

The Master Read Address Register is continually updated during the transfer process and will always be pointing to the next unread location. Reading of this register during a transfer process (done when the S5933 controller is functioning as a target i.e., not a bus master) is permitted and may be used to monitor the progress of the transfer.

During the address phase for bus master read transfers, the two least significant bits presented on the PCI bus AD[31:0] will always be zero. This identifies to the target memory that the burst address sequence will be in a linear order rather than in an Intel 486 or Pentium™ cache line fill sequence. Also, the PCI bus address bit A1 will always be zero when this controller is the bus master. This signifies to the target that the controller is burst capable and that the target should not arbitrarily disconnect after the first data phase of this operation.

DSP controlled bus master write transfer count register (MWTC)

The master write transfer count register is used to convey to the S5933 controller the actual number of bytes that are to be transferred. *TORNADO-Pxxxx* on-board DSP can read/write to this register, since *TORNADO-Pxxxx* DSP systems are configured to use DSP controlled (Add-On initiated) PCI-bus mastering.

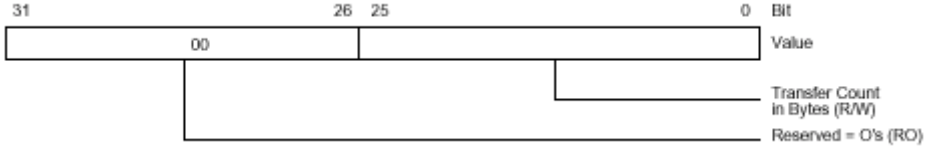


Fig. B-12. Add-On Controlled Bus Master Write Transfer Count Register

The value in this register is decremented with each bus master PCI write operation until the transfer count reaches zero. Upon reaching zero, the transfer operation ceases and an interrupt may be optionally generated to either the PCI bus or DSP. Transfers which are not whole multiples of DWORDs in size result in a partial word ending cycle. This partial word ending cycle is possible since all bus master transfers for this controller are required to begin on a DWORD boundary.

DSP controlled bus master read transfer count register (MRTC)

The master read transfer count register is used to convey to the PCI controller the actual number of bytes that are to be transferred. *TORNADO-Pxxxx* on-board DSP can read/write to this register, since *TORNADO-Pxxxx* DSP systems are configured to use DSP controlled (Add-On initiated) PCI-bus mastering.

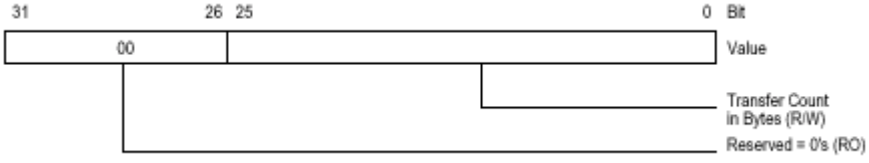


Fig. B-13. Add-On Controlled Bus Master Read Transfer Count Register

The value in this register is decremented with each bus master PCI read operation until the transfer count reaches zero. Upon reaching zero, the transfer operation ceases and an interrupt may be optionally generated to either the PCI bus or DSP. Transfers which are not whole multiples of DWORDs in size result in a partial word ending cycle. This partial word ending cycle is possible since all bus master transfers for this controller are required to begin on a DWORD boundary.

Add-on (DSP) mailbox empty/full status register (AMBEF)

This register provides empty/full visibility of each byte within the mailboxes. The empty/full status for the Outgoing mailboxes are displayed on the high order 16 bits and the empty/full status for the incoming mailboxes are presented on the low order 16 bits.

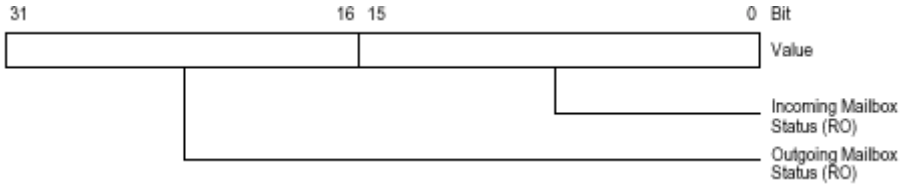


Fig. B-14. Add-On Mailbox Empty/Full Status Register

Table B-6. Add-On Mailbox Empty/Full Status Register

Bit	Description
31:16	Outgoing Mailbox Status. This field indicates which outgoing mailbox registers have been written by the Add-On bus interface but have not yet been read by the PCI bus. Each bit location corresponds to a specific byte within one of the four outgoing mailboxes. A value of one for each bit signifies that the specified mailbox byte is full, a value of zero signifies empty. The mapping of these status bits to bytes within each mailbox is as follows: Bit 31 = Outgoing mailbox 4 byte 3 Bit 30 = Outgoing mailbox 4 byte 2 Bit 29 = Outgoing mailbox 4 byte 1 Bit 28 = Outgoing mailbox 4 byte 0 Bit 27 = Outgoing mailbox 3 byte 3 Bit 26 = Outgoing mailbox 3 byte 2 Bit 25 = Outgoing mailbox 3 byte 1 Bit 24 = Outgoing mailbox 3 byte 0 Bit 23 = Outgoing mailbox 2 byte 3 Bit 22 = Outgoing mailbox 2 byte 2 Bit 21 = Outgoing mailbox 2 byte 1 Bit 20 = Outgoing mailbox 2 byte 0 Bit 19 = Outgoing mailbox 1 byte 3 Bit 18 = Outgoing mailbox 1 byte 2 Bit 17 = Outgoing mailbox 1 byte 1 Bit 16 = Outgoing mailbox 1 byte 0
15:00	Incoming Mailbox Status. This field indicates which incoming mailbox registers have been written by the PCI bus but not yet been read by the Add-On interface. Each bit location corresponds to a specific byte within one of the four incoming mailboxes. A value of one for each bit signifies that the specified mailbox byte is full, a value of zero signifies empty. The mapping of these status bits to bytes within each mailbox is as follows: Bit 15 = Incoming mailbox 4 byte 3 Bit 14 = Incoming mailbox 4 byte 2 Bit 13 = Incoming mailbox 4 byte 1 Bit 12 = Incoming mailbox 4 byte 0 Bit 11 = Incoming mailbox 3 byte 3 Bit 10 = Incoming mailbox 3 byte 2 Bit 9 = Incoming mailbox 3 byte 1 Bit 8 = Incoming mailbox 3 byte 0 Bit 7 = Incoming mailbox 2 byte 3 Bit 6 = Incoming mailbox 2 byte 2 Bit 5 = Incoming mailbox 2 byte 1 Bit 4 = Incoming mailbox 2 byte 0 Bit 3 = Incoming mailbox 1 byte 3 Bit 2 = Incoming mailbox 1 byte 2 Bit 1 = Incoming mailbox 1 byte 1 Bit 0 = Incoming mailbox 1 byte 0

A value of one signifies that a given mailbox had been written by the sourcing interface but had not yet been read by the corresponding destination interface. An incoming mailbox is defined as one in which data travels from the PCI bus into the DSP environment and an outgoing mailbox is defined as one where data goes OUT from the DSP to the PCI interface.

Add-on (DSP) interrupt control/status register (AINT)

This register provides the method for choosing which conditions are to produce an interrupt from PCIC to *TORNADO-Pxxxx* on-board DSP, a method for viewing the cause for the interrupt, and a method for acknowledging (removing) the interrupt's assertion.

Available Interrupt sources:

- one of the incoming mailboxes (1,2,3 or 4) becomes full
- one of the outgoing mailboxes (1,2,3 or 4) becomes empty
- built-in self test issued.
- write transfer count is zero
- read transfer count is zero
- target/master Abort.

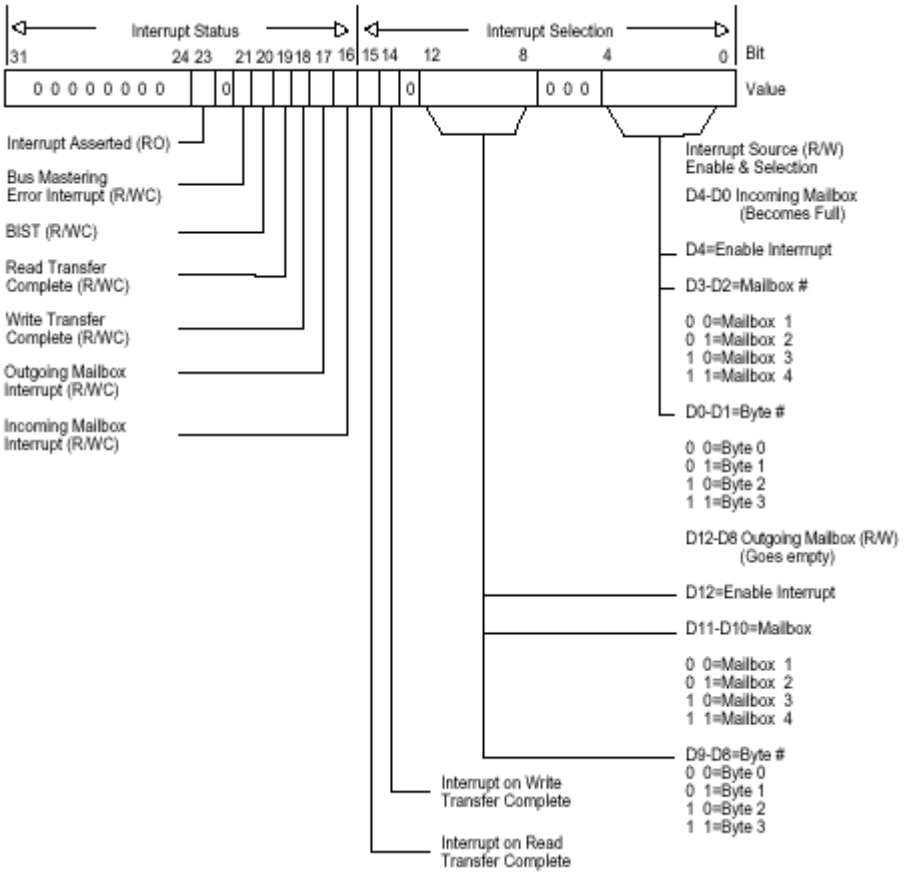


Fig. B-15. Add-On Interrupt Control/Status Register

Table B-7. Interrupt Control/Status Register

Bit	***Description***
31:24	Reserved. Always zero.
23	Interrupt asserted. This read-only status bit indicates that one or more interrupt conditions is present. This bit is nothing more than the ORing of the interrupt conditions described by bits, 20, 17 and 16 of this register.
22	Reserved. Always zero.
21	Master/Target Abort. This bit signifies that an interrupt has been generated due to the S5933 encountering a Master or Target abort during an S5933 initiated PCI bus cycle. This bit operates as read or write one clear. Writing a one to this bit causes it to be cleared. Writing a zero to this bit does nothing.
20	BIST. Built-In Self-Test interrupt. This interrupt occurs when a self test is initiated by the PCI interface writing of the BIST configuration register. This bit will stay set until cleared by writing a one to this location. Self test completion codes may be passed to the PCI BIST register by writing to the AGCSTS register described in the corresponding subsection below. This bit is generally not required for use in *TORNADO-Pxxxx* DSP systems.
19	Read Transfer Complete. This bit signifies that an interrupt has been generated due to the completion of a PCI bus master operation involving the transfer of data from the PCI bus to the DSP. This interrupt will occur when the Master Read Transfer Count register reaches zero. This bit operates as read or write one clear. A write to this bit with the data of one will cause this bit to be reset; a write to this bit with the data of zero will not change the state of this bit.
18	Write Transfer Complete. This bit signifies that an interrupt has been generated due to the completion of a PCI bus master operation involving the transfer of data to the PCI bus from the DSP. This interrupt will occur when the Master Write Transfer Count register reaches zero. This bit operates as read or write one clear. A write to this bit with the data of one will cause this bit to be reset; a write to this bit with the data of zero will not change the state of this bit.
17	Outgoing Mailbox Interrupt. This bit sets when the mailbox selected by bits 12 through 8 of this register is read by the PCI interface. This bit operates as read or write one clear. A write to this bit with the data as one will cause this bit to be reset; a write to this bit with the data as zero will not change the state of this bit.
16	Incoming Mailbox Interrupt. This bit sets when the mailbox selected by bits 5 through 0 of this register are written by the PCI interface. This bit operates as read or write one clear. A write to this bit with the data of one will cause this bit to be reset; a write to this bit with the data as zero will not change the state of this bit.
15	Interrupt on Read Transfer Complete. This bit enables the occurrence of an interrupt when the read transfer count reaches zero. This bit is read/write.
14	Interrupt on Write Transfer Complete. This bit enables the occurrence of an interrupt when the write transfer count reaches zero. This bit is read/write.
13	Reserved. Always zero.
12	Enable outgoing mailbox interrupt. This bit allows a read by the PCI of the outgoing mailbox register identified by bits 11 through 8 to produce an PCIC-to-DSP (AOB) interrupt. This bit is read/write.

11:10	Outgoing Mailbox Interrupt Select. This field selects which of the four outgoing mailboxes is to be the source for causing an outgoing mailbox interrupt. This field is read/write.
9:8	Outgoing Mailbox Byte Interrupt select. This field selects which byte of the mailbox selected by bits 11 and 10 above is to actually cause the interrupt. This field is read/write.
7:5	Reserved. Always zero.
4	Enable incoming mailbox interrupt. This bit allows a write from the PCI bus to the incoming mailbox register identified by bits 3 through 0 to produce an PCIC-to-DSP (AOB) interrupt. This bit is read/write.
3:2	Incoming Mailbox Interrupt Select. This field selects which of the four incoming mailboxes is to be the source for causing an incoming mailbox interrupt. This field is read/write.
1:0	Incoming Mailbox Byte Interrupt select. This field selects which byte of the mailbox selected by bits 3 and 2 above is to actually cause the interrupt.

Add-on (DSP) general control/status register (AGCSTS)

This register provides for overall control of the AMCC S5933 PCIC on-chip AOB operation registers. It is used to provide a method to perform software resets of the mailbox and FIFO flags, to access EEPROM/nvRAM from DSP application, and to start/stop DSP controlled PCI-bus mastering data transfers.

The following controls are provided:

- reset PCI-to-DSP (PCI to Add-On) FIFO flags
- reset DSP-to-PCI (Add-On to PCI) FIFO flags
- reset mailbox empty full status flags
- write/read external non-volatile memory
- PCI-bus mastering data transfer count enable.

The following status flags are provided:

- DSP-to-PCI (Add-On to PCI) FIFO full
- DSP-to-PCI (Add-On to PCI) FIFO has four or more empty locations
- DSP-to-PCI (Add-On to PCI) FIFO empty
- PCI-to-DSP (PCI to Add-On) FIFO full
- PCI-to-DSP (PCI to Add-On) FIFO has four or more words loaded
- PCI-to-DSP (PCI to Add-On) FIFO empty.

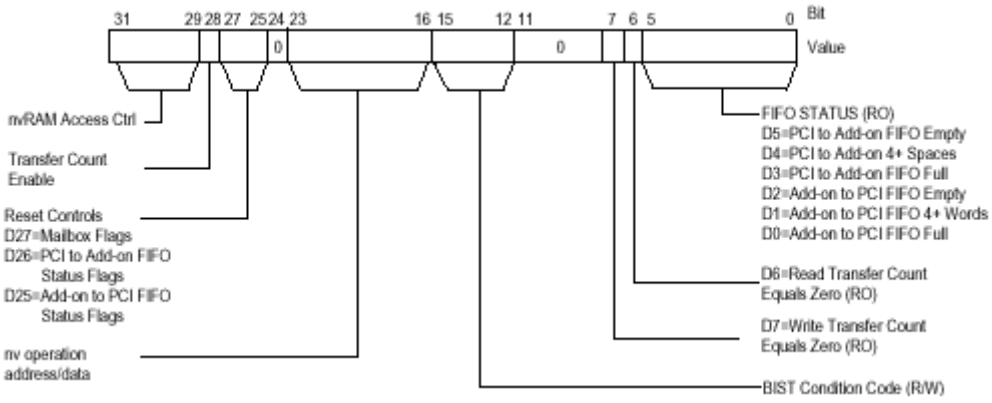


Fig. B-16. Add-On General Control/Status Register

Table B-8. Add-On General Control/Status Register

Bit	***Description***
31:29	nvRAM/EPROM Access Control from DSP application. This field provides a method for access to the optional, external non-volatile memory. Write operations are achieved by a sequence of byte operations involving these bits and the 8-bit field of bits 23 through 16. The sequence requires that the low-order address, high-order address, and then a data byte be loaded in order. Bit 31 of this field acts as an enable/clock and ready for the access to the external memory. D31 must be written to a 1 before an access can begin, and subsequent accesses must wait for bit D31 to become zero (ready). *D31* *D30* *D29* *W/R* *function* 0 X X W Inactive 1 0 0 W Load low address byte 1 0 1 W Load high address byte 1 1 0 W Begin write 1 1 1 W Begin read 0 X X R Ready 1 X X R Busy Cautionary note: The non-volatile memory interface is also available for access by the PCI bus interface. Accesses by both the Add-On and PCI bus to the nvRAM are not directly supported by this component. Software must be designed to prevent the simultaneous access of nvRAM to prevent data corruption within the memory and provide for accurate data retrieval.
28	Transfer Count Enable. When set, transfer counts are used for DSP (Add-On) initiated bus master transfers. When clear, transfer counts are ignored, which can be useful to pause DSP controlled PCI-bus mastering procurement.
27	Mailbox Flag Reset. Writing a 1 to this bit causes all mailbox status flags to become reset (EMPTY). It is not necessary to write this bit as 0 because it is used internally to produce a reset pulse. Since reading of this bit will always produce zeros, this bit is write only.

26	PCI-to-DSP (PCI to Add-On) FIFO Status Reset. Writing a 1 to this bit causes the Inbound (Bus master reads) FIFO empty flag to set indicating empty and the FIFO FULL flag to reset and the FIFO Four Plus spaces flag to set. It is not necessary to write this bit as 0 because it is used internally to produce a reset pulse. Since reading of this bit would always produce zeros, this bit is write only.
25	DSP-to-PCI (Add-On to PCI) FIFO Status Reset. Writing a one to this bit causes the Outbound (Bus master writes) FIFO empty flag to set indicating empty and the FIFO FULL flag to reset and the FIFO Four Plus words available flag to reset. It is not necessary to write this bit as zero because it is used internally to produce a reset pulse. Since reading of this bit would always produce zeros, this bit is write only.
24	Reserved. Always zero.
23:16	Non-volatile memory address/data port. This 8-bit field is used in conjunction with bit 31, 30 and 29 of this register to access the external non-volatile memory. The contents written are either low address, high address, or data as defined by bits 30 and 29. This register will contain the external non-volatile memory data when the proper read sequence for bits 31 through 29 is performed.
15:12	BIST condition code. This field is directly connected to the PCI configuration self test register described in Section 4.10 of AMCC S5933 PCIC User's Guide. Bit 15 through 12 maps with the BIST register bits 3 through 0, respectively.
11:8	Reserved. Always zero.
7	DSP-to-PCI Transfer Count Equal Zero during DSP controlled PCI-bus mastering (RO). This bit as a one signifies that the write transfer count is all zeros.
6	PCI-to-DSP Transfer Count Equals Zero during DSP controlled PCI-bus mastering (RO). This bit as a one signifies that the read transfer count is all zeros.
5	PCI-to-DSP (PCI to Add-on) FIFO Empty. This bit is a 1 when the PCI-to-DSP FIFO is empty.
4	PCI-to-DSP (PCI to Add-On) FIFO 4+ spaces. This bit is a 1 when there are four or more open spaces in the PCI-to-DSP FIFO.
3	PCI-to-DSP (PCI to Add-On) FIFO Full. This bit is a 1 when the PCI-to-DSP FIFO is full.
2	DSP-to-PCI (Add-on to PCI) FIFO Empty. This bit is a 1 when the DSP-to-PCI FIFO is empty.
1	DSP-to-PCI (Add-on to PCI) FIFO 4+ words. This bit is a 1 when there are four or more full locations in the DSP-to-PCI FIFO.
0	DSP-to-PCI (Add-on to PCI) FIFO Full. This bit is a 1 when the DSP-to-PCI FIFO is full.

B.4 AMCC S5933 PCIC Mailboxes Operation

This section contains description for AMCC S5933 PCIC on-chip mailbox operation, which can be useful for passing command and status information between the DSP and the PCI bus.

functional description

AMCC S5933 PCIC has eight 32-bit mailbox registers. The PCI interface and the DSP interface each have four incoming mailboxes (IMBx or AIMBx) and four outgoing mailboxes (OMBx or AOMBx) along with a single mailbox status register (MBEF or AMBEF). Outgoing mailboxes are read/write, incoming mailboxes and the mailbox status registers are read-only. Mailboxes themselves and mailbox status registers appear as the subsets of the corresponding PCI and AOB operation registers (refer to sections B.2 and B.3 for more details)

The PCI incoming and DSP outgoing mailboxes are the same, internally. The DSP incoming and PCI outgoing mailboxes are also the same, internally. The mailbox status may be monitored in two ways. The PCI and DSP interfaces each have a mailbox status register to indicate the empty/full status of bytes within the mailboxes. The mailboxes may also be configured to generate interrupts to the PCI and/or DSP interface. One outgoing and one incoming mailbox on each interface can be configured to generate interrupts.

The DSP mailbox interface behaves similar to the PCI bus interface. DSP writes to full outgoing mailboxes overwrite data currently in that mailbox. PCI reads from empty incoming mailboxes return the data that was previously contained in the mailbox. DSP incoming and outgoing mailbox interrupts are enabled in the DSP Interrupt Control/Status Register (AINT). The mailboxes can generate the PCIC-to-DSP interrupt request under two conditions (individually enabled).

DSP incoming mailbox read accesses pass through an output interlock latch. This prevents a PCI bus write to a PCI outgoing mail-box from corrupting data being read by the DSP.

PCI incoming mailbox reads also pass through an interlocking mechanism. This prevents an DSP write to an outgoing mailbox from corrupting data being read by the PCI bus. The following sections describe the mailbox flag functionality and the mailbox interrupt capabilities.

Mailbox Empty/Full Conditions

The PCI and DSP interfaces each have a mailbox status register. The PCI Mailbox Empty/Full Status (MBEF) and Add-on (DSP) Mailbox Empty/Full Status (AMBEF) Registers indicate the status of all bytes within the mailbox registers.

A write to an outgoing mailbox sets the status bits for that mailbox. The byte enables determine which bytes within the mailbox be-come full (and which status bits are set). An outgoing mailbox for one interface is an incoming mailbox for the other. Therefore, incoming mailbox status bits on one interface are identical to the corresponding outgoing mailbox status bits on the other interface.

The following list shows the relationship between the mailbox registers on the PCI and DSP interfaces.

PCI Interface		*DSP Interface*
Outgoing Mailbox 1	=	Incoming Mailbox 1
Outgoing Mailbox 2	=	Incoming Mailbox 2
Outgoing Mailbox 3	=	Incoming Mailbox 3
Outgoing Mailbox 4	=	Incoming Mailbox 4
Incoming Mailbox 1	=	Outgoing Mailbox 1
Incoming Mailbox 2	=	Outgoing Mailbox 2
Incoming Mailbox 3	=	Outgoing Mailbox 3
Incoming Mailbox 4	=	Outgoing Mailbox 4
PCI Mailbox Empty/Full	=	Add-On (DSP) Mailbox Empty/Full

A write to an outgoing mailbox also writes data into the incoming mailbox on the other interface. It also sets the status bits for the outgoing mailbox and the status bits for the incoming mailbox on the other interface. Reading the incoming mailbox clears all corresponding status bits in the Add-on and PCI mailbox status registers (AMBEF and MBEF).

For example, a PCI write is performed to the PCI outgoing mailbox 2, writing bytes 0 and 1. Reading the PCI Mailbox Empty/Full Status Register (MBEF) indicates that bits 4 and 5 are set. These bits indicate that outgoing mailbox 2, bytes 0 and 1 are full. Reading the Add-on Mailbox Empty/Full Status Register (AMBEF) shows that bits 4 and 5 in this register are also set, indicating DSP incoming mailbox 2, bytes 0 and 1 are full. An DSP read of incoming mailbox 2, bytes 0 and 1 clears the status bits in both the MBEF and AMBEF status registers. To reset individual flags in the MBEF and AMBEF registers, the corresponding byte must be read from the incoming mailbox. The PCI and Add-on mailbox status registers, MBEF and AMBEF, are read-only. Mailbox flags may be globally reset from either the PCI interface or the DSP interface. The PCI Bus Master Control/Status Register (MCSR) and the Add-on General Control/Status Register (AGCSTS) each have a bit to reset all of the mailbox status flags.

Mailbox Interrupts

The designer has the option to generate interrupts to the PCI and DSP interfaces when specific mailbox events occur.

The PCI and DSP interfaces can each define two conditions where interrupts may be generated. An interrupt can be generated when an incoming mailbox becomes full and/or when an outgoing mailbox becomes empty. A specific byte within a specific mailbox is selected to generate the interrupt. The conditions defined to generate interrupts to the PCI interface do not have to be the same as the conditions defined for the DSP interface. Interrupts must be cleared through software.

For incoming mailbox interrupts, when the specified byte becomes full, an interrupt is generated. The interrupt might be used to indicate command or status information has been provided, and must be read. For PCI incoming mailbox interrupts, the S5933 asserts the PCI interrupt. For Add-on incoming mailbox interrupts, the S5933 asserts the PCIC-to-DSP interrupt request.

For outgoing mailbox interrupts, when the specified byte becomes empty, an interrupt is generated. The interrupt might be used to indicate that the other interface has received the last information sent and more may be written. For PCI outgoing mailbox interrupts, the S5933 asserts the PCI interrupt. For Add-on outgoing mailbox interrupts, the S5933 asserts the PCIC-to-DSP interrupt request.

Add-On Outgoing Mailbox 4, Byte 3 Access

PCI incoming mailbox 4, byte 3 (Add-on outgoing mailbox 4, byte 3) does not function exactly like the other mailbox bytes in *TORNADO-Pxxxx* DSP systems and is used to generate DSP-to-PCI interrupt request from *TORNADO-Pxxxx* on-board resources of host PCI-bus interface.

Byte 3 of PCI incoming mailbox 4 (Add-on outgoing mailbox 4) is not loaded when DSP application writes to the *DSP_PCIC_OMBX3_RG* AMCC S5933 PCIC on-chip AOB operation register. Instead, byte 3 of *DSP_PCIC_OMBX3_RG* AMCC S5933 PCIC on-chip AOB operation register is loaded when the TRUE condition occurs defined by *HIF_IS_RG* and *HIF_IM_RG* HIF registers of *TORNADO-Pxxxx* host PCI-bus interface (refer to section "Host PCI-bus interface" of chapter 2 of your *TORNADO-Pxxxx* User's Guide for more details). This TRUE condition occurs each time any of the interrupt request status bits of *HIF_IS_RG* HIF register goes to the '1' state while the corresponding interrupt enable bit of *HIF_IM_RG* HIF register has been

set to the '1' state. This TRUE condition sets bit 31 of S5933 PCIC MBEF AOB operation register on the DSP side and results in setting bit 31 of MBEF PCI operation register on the PCI-bus side.

Host PCI-bus interrupt request will be generated on this TRUE condition in case PCI interrupt control/status operation register (INTCSR) is configured to generate host PCI-bus interrupt request on byte 3 of PCI incoming mailbox 4 (*HOST_PCIC_IMBX3_RG*).

processing mailbox status

Every byte in each mailbox has a status bit in the Mailbox Empty/Full Status Registers (MBEF and AMBEF). Writing a particular byte into an outgoing mailbox sets the corresponding status bit in both the MBEF and AMBEF registers. A read of a 'full' byte in a mailbox clears the status bit. The MBEF and AMBEF are read-only. Status bits cannot cleared by writes to the status registers.

The S5933 allows the mailbox status bits to be reset through software. The Bus Master Control/Status (MCSR) PCI Operation Register and the Add-on General Control/Status (AGCSTS) AOB Operation Register each have a bit to reset mailbox status. Writing a '1' to Mailbox Flag Reset bit in the MCSR or the AGCSTS register immediately clears all bits in the both the MBEF and AMBEF registers. Writing a '0' has no effect. The Mailbox Flag Reset bit is write-only. The flag bits should be monitored when transferring data through the mailboxes. Checking the mailbox status before performing an operation prevents data from being lost or corrupted. The following sequences are suggested for PCI mailbox operations using status polling (interrupts disabled):

Reading a PCI Incoming Mailbox:

1) Check Mailbox Status. Read the mailbox status register to determine if any information has been passed from the Add-On interface.

MBEF	Bits 31:16	If a bit is set, valid data is contained in the corresponding mailbox byte.

2) Read Mailbox(es). Read the mailbox bytes which MBEF indicates are full. This automatically resets the status bits in the MBEF and AMBEF registers.

IMBx	Bits 31:0	Mailbox data.

Writing a PCI Outgoing Mailbox:

1) Check Mailbox Status. Read the mailbox status register to determine if information previously written to the mailbox has been read by the Add-On interface. Writes to full mailbox bytes overwrite data currently in the mailbox (if not already read by the Add-On interface). Repeat until the byte(s) to be written are empty.

MBEF	Bits 15:0	If a bit is set, valid data is contained in the corresponding mailbox byte and has not been read by the Add-On.

2) Write Mailbox(es). Write to the outgoing mailbox byte(s).

OMBx	Bits 31:0	Mailbox data.

Mailbox operations for the DSP interface are functionally identical. The following sequences are suggested for DSP mailbox operations using status polling (interrupts disabled):

Reading an Add-On Incoming Mailbox:

1) Check Mailbox Status. Read the mailbox status register to determine if any information has been passed from the PCI interface.

AMBEF	Bits 15:0	If a bit is set, valid data is contained in the corresponding mailbox byte.

2) Read Mailbox(es). Read the mailbox bytes which AMBEF indicates are full. This automatically resets the status bits in the AMBEF and MBEF registers.

AIMBx	Bits 31:0	Mailbox data.

Writing an Add-On Outgoing Mailbox:

1) Check Mailbox Status. Read the mailbox status register to determine if information previously written to the mailbox has been read by the PCI interface. Writes to full mailbox bytes overwrite data currently in the mailbox (if not already read by the PCI interface). Repeat until the byte(s) to be written are empty.

AMBEF	Bits 31:16	If a bit is set, valid data is contained in the corresponding mailbox byte and has not been read by the PCI bus.

2) Write Mailbox(es). Write to the outgoing mailbox byte(s).

AOMBx	Bits 31:0	Mailbox data.

generating mailbox interrupts

Although polling status is useful, in some cases, polling requires continuous actions by the processor reading or writing the mailbox. Mailbox interrupt capabilities are provided to avoid much of the processor overhead required by continuously polling status bits. The DSP and PCI interface can each generate interrupts on an incoming mailbox condition and/or an outgoing mailbox condition. These can be individually enabled/disabled. A specific byte in one incoming mailbox and one outgoing mailbox is identified to generate the interrupt(s). The tasks required to setup mailbox interrupts are shown below:

Enabling PCI mailbox interrupts:

1) Enable PCI outgoing mailbox interrupts. A specific byte within one of the outgoing mailboxes is identified to assert INTA# when read by the Add-On interface.

INTCSR	Bit 4	Enable outgoing mailbox interrupts
INTCSR	Bits 3:2	Identify mailbox to generate interrupt
INTCSR	Bits 1:0	Identify mailbox byte to generate interrupt

2) Enable PCI incoming mailbox interrupts. A specific byte within one of the incoming mailboxes is identified to assert INTA# when written by the Add-On interface.

INTCSR	Bit 12	Enable incoming mailbox interrupts
INTCSR	Bits 11:10	Identify mailbox to generate interrupt
INTCSR	Bits 9:8	Identify mailbox byte to generate interrupt

Enabling Add-On mailbox interrupts:

1) Enable Add-On outgoing mailbox interrupts. A specific byte within one of the outgoing mailboxes is identified to assert IRQ# when read by the PCI interface.

AINT	Bit 12	Enable outgoing mailbox interrupts
AINT	Bits 11:10	Identify mailbox to generate interrupt
AINT	Bits 9:8	Identify mailbox byte to generate interrupt

2) Enable Add-On incoming mailbox interrupts. A specific byte within one of the incoming mailboxes is identified to assert IRQ# when written by the PCI interface.

AINT	Bit 4	Enable incoming mailbox interrupts
AINT	Bits 3:2	Identify mailbox to generate interrupt
AINT	Bits 1:0	Identify mailbox byte to generate interrupt

With either the Add-On or PCI interface, these two steps can be performed with a single access to the appropriate register. They are shown separately here for clarity.

Once interrupts are enabled, the interrupt service routine must access the mailboxes and clear the interrupt source. A particular application may not require all of the steps shown. For instance, a design may only use incoming mailbox interrupts and not require support for outgoing mailbox interrupts. The interrupt service routine tasks are shown below:

Servicing a PCI mailbox interrupt (INTA#):

1) Identify the interrupt source(s). Multiple interrupt sources are available on the S5933. The interrupt service routine must verify that a mailbox generated the interrupt (and not some other interrupt source).

INTCSR	Bit 16	PCI outgoing mailbox interrupt indicator
INTCSR	Bit 17	PCI incoming mailbox interrupt indicator

2) Check mailbox status. The mailbox status bits indicate which mailbox bytes must be read or written.

MBEF	Bits 31:16	Full PCI incoming mailbox bytes
MBEF	Bits 15:0	Empty PCI outgoing mailbox bytes

3) Access the mailbox. Based on the contents of MBEF, mailboxes are read or written. Reading an incoming mailbox byte clears the corresponding status bit in MBEF.

OMBx	Bits 31:0	PCI outgoing mailboxes
IMBx	Bits 31:0	PCI incoming mailboxes

4) Clear the interrupt source. The PCI INTA# signal is deasserted by clearing the interrupt request. The request is cleared by writing a '1' to the appropriate bit.

INTCSR	Bit 16	Clear PCI outgoing mailbox interrupt
INTCSR	Bit 17	Clear PCI incoming mailbox interrupt

Servicing an Add-On mailbox interrupt (IRQ#):

1) Identify the interrupt source(s). Multiple interrupt sources are available on the S5933. The interrupt service routine must verify that a mailbox generated the interrupt (and not some other interrupt source).

AINT	Bit 16	Add-On incoming mailbox interrupt indicator
AINT	Bit 17	Add-On outgoing mailbox interrupt indicator

2) Check mailbox status. The mailbox status bits indicate which mailbox bytes must be read or written.

AMBEF	Bits 31:16	Empty Add-On outgoing mailbox bytes
AMBEF	Bits 15:0	Full Add-On incoming mailbox bytes

3) Access the mailbox. Based on the contents of AMBEF, mailboxes are read or written. Reading an incoming mailbox byte clears the corresponding status bit in AMBEF.

AIMBx	Bits 31:0	Add-On incoming mailboxes
AOMBx	Bits 31:0	Add-On outgoing mailboxes

4) Clear the interrupt source. The Add-On IRQ# signal is deasserted by clearing the interrupt request. The request is cleared by writing a '1' to the appropriate bit.

AINT	Bit 16	Clear Add-On incoming mailbox interrupt
AINT	Bit 17	Clear Add-On outgoing mailbox interrupt

In both cases, step 3 involves accessing the mailbox. To allow the incoming mailbox interrupt logic to be cleared, the mailbox status bit must also be cleared. Reading an incoming mailbox clears the status bits. Another option for clearing the status bits is to use the Mailbox Flag Reset bit in the MCSR and AGCSTS registers, but this clears all status bits, not just for a single mailbox or mailbox byte. For outgoing mailbox interrupts, the read of a mailbox register is what generated the interrupt; this ensures the status bits are already clear.

B.5 AMCC S5933 PCIC FIFO Operation and DSP Controlled PCI-bus Mastering

This section contains description for AMCC S5933 PCIC on-chip FIFO operation, which can be useful for 'stream'-type bidirectional data transfer between host PCI-bus and *TORNADO-Pxxxx* on-board DSP environment and is also used as the data path during DSP controlled PCI-bus mastering data transfers.

General information

The S5933 has two internal FIFOs. One FIFO is for PCI bus to DSP environment, the other FIFO is for DSP environment to PCI bus transfers. Each of these has eight 32-bit registers. The FIFOs are both addressed as a single PCI and AOB Operation Register from both PC and DSP applications, but which internal FIFO is accessed is determined by whether the access is a read or write.

FIFO control and status indicators allow a simple FIFO access from host PC and DSP applications. The following section describes FIFO control in details.

The FIFO may be either a PCI target or a PCI initiator. As a target, the FIFO allows a PCI bus master to access DSP data. The FIFO also allows the S5933 to become a PCI initiator. Read and write address registers and transfer count registers allow the S5933 to perform DMA transfers across the PCI bus. The FIFO may act as initiator and a target at different times in the same application. PCI-bus and PCIC-to-DSP interrupt capabilities are available to support bus mastering through the FIFO.

The S5933 FIFO interface allows a high degree of functionality and flexibility. Applications may implement the FIFO as either a PCI target or program it to enable the S5933 to be a PCI initiator (bus master). The following sections describe, on a functional level, the capabilities of the S5933 FIFO interface.

FIFO PCI Interface (Target Mode)

The S5933 FIFO may act as a standard PCI target. FIFO empty/full status may be determined by the PCI initiator by reading the status bits in the PCI Bus Master Control/Status PCI operation Register (MCSR).

The FIFO occupies a single 32-bit register location within the PCI Operation Registers. A PCI initiator may not perform burst accesses on the FIFO. Each data phase of a burst causes the PCI initiator to increment its address counter (even though only the first address is driven at the beginning of the burst). The initiator keeps track of the current address in case a disconnect occurs. This allows the initiator to continue the burst from where the disconnect occurred. If the S5933 FIFO initiated a disconnect during a PCI burst to the FIFO register, the burst would be resumed at an address other than the FIFO location (because the initiator address counter has incremented). The S5933 always signals a disconnect if a burst to any PCI Operation Register is attempted. Because the PCI-to-DSP (PCI to Add-On) FIFO and the DSP-to-PCI (Add-On to PCI) FIFO occupy a single location within the PCI and Add-On Operation Registers, which FIFO is accessed is determined by whether the access is a read or write. This means that once data is written into the FIFO, the value written cannot be read back.

For PCI reads from the DSP-to-PCI (Add-On to PCI) FIFO, the S5933 completes the PCI cycle. If the PCI bus attempts to read an empty FIFO, the S5933 immediately issues a disconnect with retry. The DSP-to-PCI (Add-On to PCI) FIFO status indicators change one PCI clock after a PCI read.

For PCI writes to the PCI-to-DSP FIFO, the S5933 completes the PCI cycle. If the PCI bus attempts to write a full FIFO, the S5933 immediately issues a disconnect with retry. The PCI-to-DSP (PCI to Add-On) FIFO status indicators change one PCI clock after a PCI write.

FIFO PCI Interface (Initiator Mode)

The S5933 can act as an initiator on the PCI bus. This allows the device to gain control of the PCI bus to transfer data to or from the FIFO. Internal address and transfer count registers control the number of PCI transfers and the locations of the transfers. The following paragraphs assume the proper registers and bits are programmed to enable bus mastering .

PCI read and write transfers from the S5933 are very similar. The FIFO management scheme (refer to the corresponding subsection below) determines when the S5933 asserts its PCI bus request. When PCI-bus grant is returned, the device begins running PCI cycles. Once the S5933 controls the bus, the FIFO management scheme is not important. It only determines when PCI bus control is initially requested. PCI bus reads and writes are always performed as bursts by the S5933, if possible.

FIFO advance control and endian conversion

The S5933 provides a high degree of flexibility for controlling the data flow through the FIFO. Each FIFO (PCI-to-DSP (PCI to Add-On) and DSP-to-PCI (Add-On to PCI)) has a specific FIFO advance condition. For FIFO writes, the byte which signifies a location is full is configurable. For FIFO reads, the byte which signifies a location is empty is configurable. This ability is useful for transferring data through the FIFO with DSP, which are not 32-bits wide.

The specific byte lane used to advance the FIFO, when accessed, is determined individually for each FIFO interface (PCI and DSP). The control bits to set the advance condition are D29:26 of the Interrupt Control/Status Register (INTCSR) in the PCI Operation Registers (refer to fig.B-7).

The default FIFO advance condition is set to byte 0 (least significant byte). With the default setting, a write of byte 0 to the FIFO asserted indicates that the FIFO location is now full, advancing the FIFO pointer to the next location. Byte 0 does not have to be the only byte enable asserted. Note, the FIFO advance condition may be different for the PCI-to-DSP (PCI to Add-On) FIFO and the DSP-to-PCI (Add-On to PCI) FIFO directions.

CAUTION

Host PC application must configure *HOST_PCIC_INTCSR_RG* AMCC S5933 PCIC on-chip PCI operation register of *TORNADO-Pxxxx* host PCI-bus interface with bits 24..31 set to default 00H state.

It is recommended that host PC application will access *HOST_PCIC_FIFO_RG* AMCC S5933 PCIC on-chip PCI operation register of *TORNADO-Pxxxx* host PCI-bus interface as 32-bit DWORD.

It is recommended that DSP application will access *DSP_PCIC_FIFO_RG* AMCC S5933 PCIC on-chip AOB operation register of *TORNADO-P6x* DSP system as 32-bit DWORD.

TORNADO-P3x on-board DSP always accesses *DSP_PCIC_FIFO_RG* AMCC S5933 PCIC on-chip AOB operation register as 32-bit DWORD.

FIFO Status and Control Bits

The FIFO status can be monitored and the FIFO operation controlled from the MCSR PCI Operation Register on the PC side and via the AGCSTS Add-On Operation Register on the DSP side.

The Bus Master Control/Status (MCSR) PCI Operation register allows a PCI host to monitor FIFO activity and control FIFO operation. Reset controls allow the PCI-to-DSP (PCI to Add-on) FIFO and DSP-to-PCI (Add-on to PCI) FIFO flags to be reset (individually). Status bits indicate if the PCI-to-DSP (PCI to Add-on) FIFO is empty, has four or more open spaces, or is full. Status bits also indicate if the DSP-to-PCI (Add-on to PCI) FIFO is empty, has four or more full locations or is full. Finally, FIFO PCI bus mastering is monitored/controlled though this register (refer to the corresponding subsection below).

The Add-On General Control/Status (AGCSTS) Add-On Operation Register allows DSP to monitor FIFO activity and control FIFO operation. Reset controls allow the PCI-to-DSP (PCI to Add-on) FIFO and DSP-to-PCI (Add-on to PCI) FIFO flags to be reset (individually). Status bits indicate if the PCI-to-DSP (PCI to Add-on) FIFO is empty, has four or more open spaces, or is full. Status bits also indicate if the DSP-to-PCI (Add-on to PCI) FIFO is empty, has four or more full spaces or is full. FIFO bus mastering status may be monitored through this register.

PCI FIFO Status Indicators

The PCI-bus implements FIFO status indicators via bits 0..5 of *HOST_PCIC_MCSR_RG* AMCC S5933 PCIC on-chip PCI operation register (refer to fig.B-9). The following FIFO indicators are provided:

- PCI-to-DSP FIFO empty indicator
- PCI-to-DSP FIFO full indicator
- DSP-to-PCI FIFO empty indicator
- DSP-to-PCI FIFO full indicator
- PCI-to-DSP FIFO 4+spaces indicator
- DSP-to-PCI FIFO 4+words indicator.

Add-On (DSP) FIFO Status Indicators

The DSP environment of *TORNADO-Pxxxx* DSP systems implements FIFO status indicators in either of the following ways:

- via bits 0..5 of *DSP_PCIC_AGCSTS_RG* AMCC S5933 PCIC on-chip AOB operation register (refer to fig.B-16)
- via *DSP_FIFO_STAT_RG* IOX register (refer to section "TMS320xxxx DSP Environment" of Chapter 2 of your *TORNADO-Pxxxx* User's Guide for more details).

Both registers actually provide identical FIFO status information except for the *DSP_PCIC_AGCSTS_RG* AMCC S5933 PCIC on-chip AOB operation register optionally provides FIFO half-full indicators. However, the main important difference between these registers is that *DSP_FIFO_STAT_RG* IOX register is accessed much faster without wait states on the DSP side.

The following FIFO indicators are provided through *DSP_PCIC_AGCSTS_RG* AMCC S5933 PCIC on-chip AOB operation register and *DSP_FIFO_STAT_RG* IOX register from the DSP environment:

- PCI-to-DSP FIFO empty indicator
- PCI-to-DSP FIFO full indicator
- DSP-to-PCI FIFO empty indicator
- DSP-to-PCI FIFO full indicator
- PCI-to-DSP FIFO 4+spaces indicator (available via *DSP_PCIC_AGCSTS_RG* AMCC S5933 PCIC on-chip AOB operation register only)
- DSP-to-PCI FIFO 4+words indicator (available via *DSP_PCIC_AGCSTS_RG* AMCC S5933 PCIC on-chip AOB operation register only).

PCI Bus Mastering with the FIFO

The S5933 may initiate PCI bus cycles through the FIFO interface. The S5933 allows blocks of data to be transferred to and from the DSP by specifying a source/destination address on the PCI bus and a transfer byte count. This DMA capability allows data to be transferred across the PCI bus without host CPU intervention. Initiating a bus master transfer requires programming the appropriate address registers and transfer byte counts.

CAUTION

TORNADO-Pxxxx on-board AMCC S5933 PCIC is configured for DSP controlled (AOB initiated) PCI bus mastering data transfers, which allow to configure and control PCI-bus mastering data transfers directly from on-board DSP application.

Initiating bus master transfers from DSP is advantageous because the host CPU does not have to intervene for the S5933 to become a PCI Initiator. At the end of a transfer the S5933 may generate an interrupt to either the PCI bus (for PCI initiated transfers) or DSP interface.

Add-On (DSP) Initiated Bus Mastering

Since *TORNADO-Pxxxx* on-board AMCC S5933 PCIC is configured for DSP controlled (AOB initiated) PCI bus mastering data transfers, then the Master Read Address Register (MRAR), Master Write Address Register (MWAR), Master Read Transfer Count (MRTC), and Master Write Transfer Count (MWTC) are accessible for read/write only from the DSP (Add-On interface) side.

CAUTION

For DSP (Add-On) initiated bus mastering for *TORNADO-Pxxxx* DSP systems, bits 10 and 14 bits of S5933 Bus Master Control/Status PCI operation Register (MCSR) are ignored, and PCI-bus mastering data transfers are controlled via *AMR_EN* and *AMW_EN* bits of *DSP_AMWREN_RG* IOX register of the DSP environment in case *AM_EN* bit of *HIF_CONTROL_RG* HIF register of *TORNADO-Pxxxx* host PCI-bus interface is set to the '1' state by host PC application in order to enable PCI-bus mastering data transfer.

Bit *AM_EN* of *HIF_CONTROL_RG* HIF register of *TORNADO-Pxxxx* host PCI-bus interface is used to disable unauthorized PCI-bus mastering data transfers, which can unexpectedly occur due to execution of invalid (incorrect) DSP code in case either on-board DSP is released from the 'RESET' state without prior loading valid DSP code, or in case DSP application has branched to invalid (incorrect) DSP code while debugging DSP application.

Refer to sections "TMS320xxxx DSP Environment" and "Host PCI-bus Interface" of Chapter 2 from your *TORNADO-Pxxxx* User's Guide for more details.

Once configured for the DSP (Add-On) initiated bus mastering, the S5933 transfers data until the transfer count reaches zero, or it may be configured to ignore the transfer count. For bus master transfers initiated by DSP, some applications may not know the size of the data block to be transferred. To avoid constantly updating the transfer count register, the transfer count may be disabled. Bit 28 in the Add-On General Control/Status Register (AGCSTS) performs this function. Disabling the transfer count also disables the interrupt capabilities.

Regardless of whether Add-On transfer count is enabled or disabled, the *AMR_EN* and *AMW_EN* bits of *DSP_AMWREN_RG* IOX register of the DSP environment and *AM_EN* bit of *HIF_CONTROL_RG* HIF register of *TORNADO-Pxxxx* host PCI-bus interface control when the S5933 asserts or deasserts its request to the PCI bus during PCI-to-DSP and DSP-to-PCI PCI-bus mastering data transfers correspondingly. When Add-

On transfer count is enabled, the S5933 will only request the bus when both the transfer count (read or write) is not zero and the appropriate enable bits (*AMR_EN* and *AMW_EN* bits of *DSP_AMWREN_RG* IOX register and *AM_EN* bit of *HIF_CONTROL_RG* HIF register) are active.

Address and Transfer Count Registers

The S5933 has two sets of registers used for bus master transfers. There are two operation registers for PCI-bus master read operations and two operation registers for PCI-bus master write operations. One operation register is for the transfer address (MWAR and MRAR). The other operation register is for the transfer byte count (MWTC and MRTC). Refer to section B.3 for details about MWAR, MRAR, MWTC and MRTC AOB operation registers formats.

The address registers are written with the first address of the transfer before bus mastering is enabled. Once a transfer begins, this register is automatically updated to reflect the address of the current transfer. If a PCI target disconnects from an S5933 initiated cycle, the transfer is retried starting from the current address in the register. If bus PCI bus grant is removed or bus mastering is disabled (via *AMR_EN* and *AMW_EN* bits of *DSP_AMWREN_RG* IOX register and *AM_EN* bit of *HIF_CONTROL_RG* HIF register), the value in the address register reflects the next address to be accessed. Transfers must begin on DWORD boundaries.

The transfer count registers contain the number of bytes to be transferred. The transfer count may be written before or after bus mastering is enabled. If bus mastering is enabled, no transfer occurs until the transfer count is programmed with a non-zero value. Once a transfer begins, this register is automatically updated to reflect the number of bytes remaining to be transferred. If the transfer count registers are disabled via bit 28 of AGCSTS AOB operation register, then transfers begin as soon as bus mastering is enabled. Although transfers must begin on DWORD boundaries, transfer counts do not have to be multiples of four bytes. For example, if the write transfer count (MWTC) register is programmed with a value of 10 (decimal), the S5933 performs two DWORD writes and a third write with only bytes 0 and 1 asserted.

Bus Mastering FIFO Management Schemes

The S5933 provides flexibility in how the FIFO is managed for PCI-bus mastering. The FIFO management scheme determines when the S5933 requests the bus to initiate PCI bus cycles. The management scheme is configurable for the PCI-to-DSP (PCI to Add-On) and DSP-to-PCI (Add-On to PCI) FIFO separately and may be different for each. PCI-bus mastering must be enabled for the management scheme to apply via *AMR_EN* and *AMW_EN* bits of *DSP_AMWREN_RG* IOX register and *AM_EN* bit of *HIF_CONTROL_RG* HIF register.

For the PCI-to-DSP (PCI to Add-On) FIFO, there are two management options. The PCI-to-DSP FIFO management option is programmed through the Bus Master Control/Status PCI operation Register (MCSR) (refer to fig B-9). The FIFO can be programmed to request the bus when any DWORD location is empty or only when four or more locations are empty. After the S5933 is granted control of the PCI bus, the management scheme does not apply. The device continues to read as long as there is an open FIFO location. When the PCI-to-DSP FIFO is full or bus mastering is disabled, the PCI bus request is removed by the S5933.

For the DSP-to-PCI (Add-On to PCI) FIFO, there are two management options. The DSP-to-PCI FIFO management option is programmed through the Bus Master Control/Status PCI operation Register (MCSR) (refer to fig B-9). The FIFO can be programmed to request the bus when any DWORD location is full or only when four or more locations are full. After the S5933 is granted control of the PCI bus, the management scheme does not apply. The device continues to write as long as there is data in the FIFO. When the DSP-to-PCI FIFO is empty or bus mastering is disabled, the PCI bus request is removed by the S5933.

There are two special cases for the DSP-to-PCI (Add-On to PCI) FIFO management scheme. The first case is when the FIFO is programmed to request the PCI bus only when four or more locations are full, but the transfer count is less than 16 bytes. In this situation, the FIFO ignores the management scheme and finishes transferring the data. The second case is when transfer count is disabled by DSP application via bit 28 of AGCSTS AOB operation register. In this situation, the FIFO management scheme must be set to request the PCI bus when one or more locations are full. *AMR_EN* and *AMW_EN* bits of *DSP_AMWREN_RG* IOX register and *AM_EN* bit of *HIF_CONTROL_RG* HIF register may be used to implement a specific FIFO management scheme.

FIFO Bus Master Cycle Priority

In many applications, the FIFO is used as a PCI initiator performing both PCI reads and writes. This requires a priority scheme be implemented.

What happens if the FIFO condition for initiating a PCI read and a PCI write are both met? Bits D12 and D8 in the Bus Master Control/Status PCI operation register (MCSR) (refer to fig B-9) control the read and write cycle priority, respectively. If these bits are both set or both clear, priority alternates, beginning with a read cycle. If the read priority is set and the write priority is clear, read cycles take priority. If the write priority is set and the read priority is clear, write cycles take priority. Priority arbitration is only done when neither FIFO has control of the PCI bus (the PCI-to-DSP FIFO would never interrupt an DSP-to-PCI FIFO transfer).

FIFO Generated Bus Master Interrupts

Interrupts may be generated under certain conditions from the FIFO during DSP controlled PCI-bus mastering data transfers for *TORNADO-Pxxxx* DSP system.

TORNADO-Pxxxx on-board PCIC-to-DSP interrupt request can be generated to on-board DSP for the following situations:

- Read transfer count reaches zero
- Write transfer count reaches zero
- An error occurred during the bus master transaction.

Refer to section "TMS320xxxx DSP Environment" of Chapter 2 from your *TORNADO-Pxxxx* User's Guide for more details about how to process PCIC-to-DSP interrupt request.

PCI-bus interrupt requests from FIFO may be generated from one or more of the following during PCI-bus mastering: read transfer count reaches zero and write transfer count reaches zero, or an error occurs during bus mastering. Error conditions include a target or master abort on the PCI bus. Interrupts on PCI error conditions are only enabled if one or both of the transfer count interrupts are enabled.

The Add-On Interrupt Control/Status Register (AINT) or the Interrupt Control Status Register (INTCSR) indicates the interrupt source for DSP and host PC applications correspondingly . The interrupt service routine may read these registers to determine what action is required. As mailboxes are also capable of generating interrupts, this must also be considered in the service routine. Interrupts are also cleared through these registers.

Along with the PCIC-to-DSP interrupt request, which can be generated to *TORNADO-Pxxxx* on-board DSP from AMCC S5933 PCIC as described above, *TORNADO-Pxxxx* DSP systems also provide two FIFO data transfer ready interrupts: interrupt requests on DSP-to-PCI FIFO and PCI-to-DSP FIFO ready conditions (refer to section "TMS320xxxx DSP Environment" of Chapter 2 from your *TORNADO-Pxxxx* User's Guide for more details). These two interrupt requests are external to TORNADO-Pxxxx on-board DSP and DSP application can configure external DSP interrupt source selectors to generate DSP external interrupt request(s) fro these sources. Once DSP external interrupt request selector is configured to generate DSP interrupt request on either of the

DSP-to-PCI FIFO and PCI-to-DSP FIFO ready conditions, then this external interrupt request can be either used to generate DSP interrupt request in order to read/write FIFO data, or can DSP application can configure DSP on-chip DMA configuration registers to generate DMA data transfer event on the corresponding FIFO ready condition. The latter is much more preferred, since DSP DMA transfers do not occupy DSP processing time and are performed concurrently with the DSP processing kernel running.

DSP controlled FIFO PCI-Bus Mastering Setup

Both *TORNADO-Pxxxx* on-board DSP and host PC applications shall perform some command sequence in order to configure and enable PCI-bus mastering data transfer(s) via AMCC S5933 PCIC correctly.

TORNADO-Pxxxx on-board DSP sets up the S5933 to perform bus master transfers. The following tasks must be completed to setup FIFO bus mastering:

1. Define transfer count abilities. Transfer counts may be either enabled or disabled. Transfer counts for read and write operations cannot be individually enabled.
    - ❑ AGCSTS Bit 28 Enable transfer count for read and write bus master transfers
2. Define interrupt capabilities. The PCI-to-DSP (PCI to Add-On) and/or DSP-to-PCI (Add-On to PCI) FIFO can generate an interrupt to the *TORNADO-Pxxxx* on-board DSP via PCI-to-DSP interrupt request when the transfer count reaches zero (if transfer counts are enabled).
    - ❑ AINT Bit 15 Enable interrupt on read transfer count equal zero
    - ❑ AINT Bit 14 Enable interrupt on write transfer count equal zero
3. Reset FIFO flags. This may not be necessary, but if the state of the FIFO flags is not known, they should be initialized.
    - ❑ AGCSTS Bit 25 Reset Add-On to PCI FIFO flags
    - ❑ AGCSTS Bit 26 Reset PCI to Add-On FIFO flags
4. Define FIFO management scheme. These bits define what FIFO condition must exist for the PCI bus request to be asserted by the S5933. This must be programmed through the PCI interface.
    - ❑ MCSR Bit 13 PCI to Add-On FIFO management scheme
    - ❑ MCSR Bit 9 Add-On to PCI FIFO management scheme
5. Define PCI-to-DSP (PCI to Add-On) and DSP-to-PCI (Add-On to PCI) FIFO priority. These bits determine which FIFO has priority if both meet the defined condition to request the PCI bus. If these bits are the same, priority alternates, with read accesses occurring first. This must be programmed through the PCI interface by host PC application.
    - ❑ MCSR Bit 12 Read vs. write priority
    - ❑ MCSR Bit 8 Write vs. read priority
6. Define transfer source/destination address. These registers are written with the first address that is to be accessed by the S5933. These address registers are updated after each access to indicate the next address to be accessed. Transfers must start on DWORD boundaries.
    - ❑ MWAR All Bus master write address
    - ❑ MRAR All Bus master read address
7. Define transfer byte counts. These registers are written with the number of bytes to be transferred. The transfer count does not have to be a multiple of four bytes. These registers are updated after each transfer to reflect the number of bytes remaining to be transferred. If transfer counts are disabled, these registers do not need to be programmed.
    - ❑ MWTC All Write transfer byte count

- MRTC All Read transfer byte count

8. Enable Bus Mastering on the host PC side. Set *AM_EN* bit of *HIF_CONTROL_RG* HIF register of *TORNADO-Pxxxx* host PCI-bus interface to the '1' state.
9. Enable and control Bus Mastering on the DSP side via bit 28 of AGCSTS PCIC on-chip AOB operation register and *AMR_EN* and *AMW_EN* bits of *DSP_AMWREN_RG* IOX register of the DSP environment. Once steps 1-8 are completed, the FIFO may operate as a PCI bus master.

Read and write bus master operation may be independently enabled or disabled. The *AMR_EN* and *AMW_EN* bits of *DSP_AMWREN_RG* IOX register of the DSP environment control bus master enabling for DSP controlled PCI-bus mastering from DSP application. Note, that the bus master enable bits of MCSR PCI-bus operation register on host PC side are ignored for *TORNADO-Pxxxx* DSP controlled PCI-bus mastering data transfers. It is recommended that bus mastering be enabled as the last step. Some applications may choose to leave bus mastering enabled via *AMR_EN* and *AMW_EN* bits of *DSP_AMWREN_RG* IOX register of the DSP environment and start transfers by writing a non-zero value to the transfer count registers (if they are enabled).

If interrupts are enabled, an PCIC-to-DSP interrupt service routine is also required. The service routine determines the source of the interrupt and resets the interrupt. As mailbox registers may also be configured to generate interrupts, the exact source of the interrupt is indicated in the Add-On Interrupt Control AOB operation Register (AINT). Typically, the interrupt service routine is used to setup the next transfer by writing new addresses and transfer counts (if enabled), but some applications may also require other actions. If read transfer or write transfer complete interrupts are enabled, the master/target abort interrupt is automatically enabled. These indicate a transfer error has occurred. Writing a one to these bits clears the corresponding interrupt.

- AINT Bit 21 Master/target abort caused interrupt
- AINT Bit 19 Read transfer complete caused interrupt
- AINT Bit 18 Write transfer complete caused interrupt

DSP application may want to use TMS320xxxx DSP on-chip DMA controller or DSP interrupt routine in order to read/write data to S5933 FIFO on the corresponding FIFO ready events rather then to use continuous FIFO ready polling in the background loop. Use DSP interrupt requests on DSP-to-PCI FIFO and PCI-to-DSP FIFO ready conditions for *TORNADO-Pxxxx* on-board DSP (refer to section "TMS320xxxx DSP Environment" of Chapter 2 from your *TORNADO-Pxxxx* User's Guide for more details). Note, that DSP on-chip DMA controlled DSP-to-FIFO and FIFO-to-DSP 'stream'-type data transfers inside DSP environment are the preferred solution, since DSP DMA transfers do not occupy DSP processing time and are performed concurrently with the DSP processing kernel running.

B.6 User Access to *TORNADO-Pxxxx* On-board Serial EEPROM/nvRAM

This section contains description for programming of *TORNADO-Pxxxx* on-board serial EEPROM/nvRAM, which is used to store start-up PCI configuration information for on-board AMCC S5933 PCIC, which is processed by PCI BIOS of host PC during PC boot procedure, and to store user-defined application specific data.

General information for TORNADO-Pxxxx on-board serial EEPROM/nvRAM

TORNADO-Pxxxx DSP systems use on-board 16kbit (2Kx8) serial EEPROM/nvRAM for start-up PCI configuration information and user-defined application specific data.

CAUTION

Only EEPROM/nvRAM locations 080H..7FFH are allowed for user access in order to store user-defined application specific data.

EEPROM/nvRAM locations 000H..07FH are not allowed for user access in any form. Modification of information in these locations may result in *TORNADO-Pxxxx* DSP system stops responding to PCI-bus requests and will be either not recognized or recognized incorrectly by PCI BIOS of host PC.

TORNADO-Pxxxx on-board serial EEPROM/nvRAM can be accessed through the PCI interface or DSP environment.

CAUTION

Care must be taken by software designers for *TORNADO-Pxxxx* DSP systems in order to exclude simultaneous access to *TORNADO-Pxxxx* on-board serial EEPROM/nvRAM simultaneously from host PC and DSP applications, since this may result in unpredictable modification of EEPROM/nvRAM contents.

Accesses to *TORNADO-Pxxxx* on-board serial EEPROM/nvRAM from the PCI interface are through the Bus Master Control/Status Register (MCSR) PCI Operation Register (refer to fig.B-9). Accesses to *TORNADO-Pxxxx* on-board serial EEPROM/nvRAM from the DSP applications are through the Add-On General Control/Status Register (AGCSTS) Add-On Operation Register (refer to fig.B15).

Accessing Non-Volatile EEPROM/nvRAM Memory

This subsection will describe how *TORNADO-Pxxxx* on-board serial EEPROM/nvRAM can be accessed from host PC application via the AMCC S5933 PCIC on-chip MCSR PCI operation register. However, provided information is also applicable for DSP accesses to *TORNADO-Pxxxx* on-board serial EEPROM/nvRAM via the AMCC S5933 PCIC on-chip AGCSTS AOB operation register.

The S5933 contains two latches within the MCSR register to control and access the nvRAM. One is an 8 bit latch called the nvRAM Address/Data Register which is used to hold nvRAM address and data information. The other is a 3 bit latch called the nvRAM Access Control Register which is used to direct the address and data information and to control the nvRAM itself.

Reading or writing to the nvRAM from host PC application is performed through bits D31:29 of AMCC S5933 PCIC on-chip MCSR register. These bits are enable and decode controls rather than a command or instruction to be executed. D31 of this register is the primary enable bit which allows all accesses to occur. When written to a ‘1’, D31 enables the decode bits D30 and D29 to direct the data contained in the address/data latch, D23:16, to

the low address, high address or data latches. D31 should be thought of as "opening a door" where as long as D31=1, then the door is open for address or data information to be altered. The table B-4 shows the D31:29 bit combinations for reading, writing, and loading address/data information. Additionally, D31 doubles as an S5933 status bit. A '1' indicates that the S5933 is currently busy reading or writing to the nvRAM. A '0' indicates a complete or inactive state.

For the examples below, we will assume the AMCC S5933 PCIC on-chip PCI operation register area of *TORNADO-Pxxxx* host PCI-bus interface is I/O mapped with the I/O base address of FC00h. These examples will read one byte to location 040H of nvRAM and write one byte to location 040H of nvRAM (this nvRAM location defines PCI-bus Vendor ID code).

This example will write 1 byte from NVRAM location 0040h and read it back:

In	**FC00h + 3Fh** (offset of NVRAM Access Control Register) until **D31 = 0** (not busy).
Out	**FC00h + 3FH** an **80h** (CMD to load the low address byte). This sets decode bits and opens door for low address latch.
Out	**FC00h + 3Eh** (offset of Address/Data Register) **40h** (the low byte of the address desired) 40h goes into latch but is not latched yet.
Out	**FC00h + 3Fh** an **A0h** (CMD to load the high address byte). This latches the low address through changing the decode bits and opens the door for the high address latch.
Out	**FC00h + 3Eh** a **00h** (the high byte of the address desired). 00h goes into the latch but is not latched yet.
Out	**FC00h + 3Fh** an **00h** (inactive CMD). This latches the high address through the disabling D31, 'closes the door'.
Out	**FC00h + 3Eh DATA** (the data byte to be written). DATA byte goes into the latch but is not latched yet.
Out	**FC00h + 3Fh** a **C0h** (CMD to write the data byte). This latches the data byte through changing the decode bits and begins to write NVRAM data operation.
In	**FC00h + 3Fh** until **D31 = 0** (not busy).
Out	**FC00h + 3Fh** an **E0h** (CMD to read the address latched).
In	**FC00h + 3Fh** until **D31 = 0** (not busy).
In	**FC00h + 3Eh** the **data.**

This example will read 1 byte from NVRAM location 0040h:

In	**FC00h + 3Fh** (offset of NVRAM Access Control Register) until **D31 = 0** (not busy).
Out	**FC00h + 3Fh** an **80h** (CMD to load the low address byte). This sets decode bits and opens door for low address latch.
Out	**FC00h + 3Eh** (offset of Address/Data Register) **40h** (the low byte of the address desired) 40h goes into latch but is not latched yet.
Out	**FC00h + 3Fh** an **A0h** (CMD to load the high address byte). This latches the low address through changing the decode bits and opens the door for the high address latch.
Out	**FC00h + 3Eh** a **00h** (the high byte of the address desired) 00h goes into latch but is not latched yet.
Out	**FC00h + 3Fh** an **E0h** (CMD to read NVRAM data). This latches the high address through changing the decode bits and begins to read the NVRAM data operation.
In	**FC00h + 3Fh** until **D31 = 0** (not busy).
In	**FC00h + 3Eh** the **data.**

This example will read 1 byte from NVRAM location 0041h and contains an extra step to demonstrate D31 operation:

In	**FC00h + 3Fh** (offset of NVRAM Access Control Register) until **D31 = 0** (not busy).
Out	**FC00h + 3Fh** an **80h** (CMD to load the low address byte). This sets decode bits and opens the door for low address latch.
Out	**FC00h + 3Eh** (offset of Address/Data Register) **40h** (the low byte of the address desired) 40h goes into latch but is not latched yet.
Out	**FC00h + 3Eh** (offset of Address/Data Register) **41h** (the low byte of the address desired) 41h goes into latch but is not latched yet.
Out	**FC00h + 3Fh** an **A0h** (CMD to load the high address byte). This latches the low address through changing the decode bits and opens the door for the high address latch.
Out	**FC00h + 3Eh 00h** (the high byte of the address desired) 00h goes into latch but is not latched yet.
Out	**FC00h + 3Fh** an **E0h** (CMD to read the address latched). This latches the high address through changing the decode bits and begins the read NVRAM data operation.
In	**FC00h + 3Fh** until **D31 = 0** (not busy).
In	**FC00h + 3Eh** the **data.**

Note, that latched addresses do not automatically increment after a read or write. They must be loaded with new values. Also, latched addresses remain after reads and writes. It is allowable to only update one address byte for the next access. Finally, host PC application may perform a one word write to load an address byte and control command simultaneously.

Appendix C. Glossary of Terms

This Glossary contains definition for terms and other synchronism used along in this databook.

A

AOB

Secondary add-on bus of AMCC S5933 PCIC (PCI Matchmaker Controller). Refer to section 2.3, , Appendix B and to original AMCC S5933 PCIC User's Guide for details.

B

Bootmode Configuration

TMS320C6x DSP bootmode. Refer to section 2.2 and table 2-2a and table 2-2b for more details.

C

D

DCM

Daughter-card module(s) for *TORNADO* DSP systems and stand-alone DSP controllers. Refer to sections 2.4 and 2.5 for more information.

DPRAM

Dual-port static RAM, which is the part of both on-board DSP environment and of host-PCI-bus interface. Refer to sections 2.2 and 2.3 for more details.

DPRAM_HM_RQ, DPRAM_MH_RQ

DPRAM memory locations, which are used for generation of PCI-to-DSP and DSP-to-PCI interrupt request correspondingly. Refer to sections 2.2 and 2.3 for more details.

DPSEM

Dual-port hardware semaphores (*TORNADO-P62xx/P67* DSP systems only). Refer to sections 2.2 and 2.3, and table 2-4 for more details.

DSP_AMWREN_RG

DSP IOX register, which is used for PCI-bus mastering control from the DSP environment. Refer to section 2.2 for more details.

DSP_DEV_ID_RG

Read-only device ID DSP IOX register (*TORNADO-P6202/P6203* DSP systems only), which must be used to identify *TORNADO* DSP system from DSP software. Refer to section 2.2 for more details.

DSP_DPRAM_IRQ

PCI-to-DSP interrupt request source via DPRAM, which is generated when host PCI-bus master writes to the DPRAM memory location *DPRAM_HM_RQ*. Refer to sections 2.2 and 2.3 for more details.

DSP_FIFO_STAT_RG

Read-only DSP IOX register, which contains current PCIC FIFO status. Refer to section 2.2 for more details.

DSP_HM_RQ0_RG, DSP_HM_RQ1_RG

Read-only DSP IOX registers (4-bit incoming DSP mailbox registers), which can be also reset by DSP and are used for generation of *HM_RQ0* and *HM_RQ1* PCI-to-PCI interrupt requests. Refer to sections 2.2 and 2.3 for more details.

DSP_MH_RQ_RG

Write-only DSP IOX register, which is used for generation of *MH_RQ* DSP-to-PCI interrupt request. Written data is ignored. Refer to section 2.2 for more details.

DSP_EXT_INT4_SEL_RG … DSP_EXT_INT7_SEL_RG

DSP IOX registers, which are used for selection of interrupt request source signals for TMS320C6x DSP external interrupt request inputs *EXT_INT4..EXT_INT7*. Refer to section 2.2 for more details.

DSP_NMI_SEL_RG

DSP IOX register, which is used for selection of interrupt request source signal for TMS320C6x DSP NMI (non-maskable interrupt request) input. Refer to section 2.2 for more details.

DSP_PCIC_AGCSTS_RG

S5933 PCIC AGCSTS AOB operation register, which is mapped to the DSP PCIC area. Refer to section 2.2, Appendix B and S5933 PCIC User's Guide for more details.

DSP_PCIC_AINT_RG

S5933 PCIC AINT AOB operation register, which is mapped to the DSP PCIC area. Refer to section 2.2, Appendix B and S5933 PCIC User's Guide for more details.

DSP_PCIC_AMBEF_RG

Read-only S5933 PCIC AMBEF AOB operation register, which is mapped to the DSP PCIC area. Refer to section 2.2, Appendix B and S5933 PCIC User's Guide for more details.

DSP_PCIC_FIFO_RG

S5933 PCIC read-FIFO and write-FIFO AOB operation registers, which are mapped to the DSP PCIC area. Refer to section 2.2, Appendix B and S5933 PCIC User's Guide for more details.

DSP_PCIC_IMBX0_RG..DSP_PCIC_IMBX3_RG

Read-only S5933 PCIC PCI-to-DSP Incoming Mailbox #1..#4 AOB operation register, which are mapped to the DSP PCIC area. Refer to section 2.2, Appendix B and S5933 PCIC User's Guide for more details.

DSP_PCIC_MRAR_RG
S5933 PCIC MRAR AOB operation register, which is mapped to the DSP PCIC area. Refer to section 2.2, Appendix B and S5933 PCIC User's Guide for more details.

DSP_PCIC_MRTC_RG
S5933 PCIC MRTC AOB operation register, which is mapped to the DSP PCIC area. Refer to section 2.2, Appendix B and S5933 PCIC User's Guide for more details.

DSP_PCIC_MWAR_RG)
S5933 PCIC MWAR AOB operation register, which is mapped to the DSP PCIC area. Refer to section 2.2, Appendix B and S5933 PCIC User's Guide for more details.

DSP_PCIC_MWTC_RG
S5933 PCIC MWTC AOB operation register, which is mapped to the DSP PCIC area. Refer to section 2.2, Appendix B and S5933 PCIC User's Guide for more details.

DSP_PCIC_OMBX0_RG.. DSP_PCIC_OMBX3_RG
S5933 PCIC DSP-to-PCI Outgoing Mailbox #1..#4 AOB operation register, which are mapped to the DSP PCIC area. Refer to section 2.2, Appendix B and S5933 PCIC User's Guide for more details.

DSP_PXSX_RESET_RG
DSP IOX register, which is used for reset control of PIOX/SIOX daughter-card sites. Refer to section 2.2 for more details.

DSP_SYS_STAT_RG
DSP IOX register, which contains information about current system configuration and which can be used for selection of external DSP memory type (*TORNADO-P6202/P6203* DSP systems only). Refer to section 2.2 for more details.

DSP_WDT_EN_RG
DSP IOX register, which is used for enable of watch-dog timer (WDT) feature. Refer to section 2.2 for more details.

DSP_WDT_CLR_RG
Write-only DSP IOX register, which is used for reset of watch-dog timer (WDT). Written data is ignored. Refer to section 2.2 for more details.

E

ECC
Emulation Controller Chip (also known as TBC), which is used for emulation control of TMS320C6x DSP via DSP on-chip JTAG port. Refer to sections 2.6 and 3.3 and to TI documentation for more

details.

EMIF_GCR, EMIF_CE0_SCR, EMIF_CE1_SCR, EMIF_CE2_SCR, EMIF_CE3_SCR
TMS320C6x DSP EMIF CE-0..CE-3 space configuration registers. Refer to section 2.2 and to TI TMS320C6x documentation for more details.

Expansion Bus
TMS320C6202/TMS320C6203 DSP expansion bus, which is used in asynchronous host port mode in *TORNADO-P6202/P6203* DSP systems in order provide 32-bit slave host port interface (HPI) feature. Refer to section 2.3 and to TI TMS320C6x documentation for more details.

EXT_INT4..EXT_INT7
TMS320C6x DSP external hardware interrupts, which are used for generation the DSP interrupts via *DSP_EXT_INT4_SEL_RG..DSP_EXT_INT7_SEL_RG* interrupt selector registers. Refer to section 2.2 and to TI TMS320C6x documentation for more details.

F

FIFO
S5933 PCIC on-chip 8-level bi-directional First-In-First-Out facility, which is used for DSP-to-PCI and PCI-to-DSP data transfers. The DSP controlled PCI-bus mastering can be used to transfer data via FIFO. Refer to sections 2.2 and 2.3, Appendix B and S5933 PCIC User's Guide for more details.

G

GPIO
General Purpose I/O. *TORNADO-P64xx* DSP systems with TMS320C64xx DSP provide on-board 10-bit DSP GPIO, which is the part of DSP on-chip peripherals. Refer to section 2.2 for more details.

H

HIF
Host Interface Registers area of *TORNADO-P6x* host PCI-bus interface. Refer to section 2.3 and to TI TMS320C6x documentation for more details.

HIF_CONTROL_RG
Host PCI-bus interface HIF register, which is used for DSP reset control and for enabling of the DSP initialised PCI-bus mastering feature. Refer to section 2.3 for more details.

HIF_CLR_DPRAM_ERR_RG

Write-only host PCI-bus interface HIF register, which is used to clear the DPRAM timeout access error. Written data is ignored. Refer to section 2.3 for more details.

HIF_CLR_HPI_ERR_RG

Write-only host PCI-bus interface HIF register, which is used to clear the HPI timeout access error. Written data is ignored. Refer to section 2.3 for more details.

HIF_CLR_MH_RQ_RG

Write-only host PCI-bus interface HIF register, which is used to clear the *MH_RQ* DSP-to-PCI interrupt request. Written data is ignored. Refer to section 2.3 for more details.

HIF_DSP_BMODE_RG

Host PCI-bus interface HIF register, which is used to set DSP bootmode in case DSP is running in host PC operation mode while DSP is in the reset state. This register is available for *TORNADO-P64xx* DSP systems only. Refer to sections 2.2 and 2.3 for more details.

HIF_HM_RQ0_RG, HIF_HM_RQ1_RG

4-bit host PCI-bus interface HIF registers, which are used for generation of PCI-to-DSP *HM_RQ0* and *HM_RQ1* interrupt requests when host PCI-bus master writes to these registers. The contents of *HIF_HM_RQ0_RG* and *HIF_HM_RQ1_RG* registers is available for read inside the DSP environment via *DSP_HM_RQ0_RG* and *DSP_HM_RQ1_RG* DSP IOX registers. DSP can also reset the contents of these registers. Refer to sections 2.2 and 2.3 for more details.

HIF_IM_RG

Host PCI-bus interface HIF register, which is used for setting individual interrupt enable masks for interrupt requests, which can generate AOB-to-PCI interrupt request via S5933 PCIC byte#3 of AOB-to-PCI incoming mailbox #4. Refer to section 2.3, Appendix B and S5933 PCIC User's Guide for more details.

HIF_IS_RG

Read-only host PCI-bus interface HIF register, which contains current status of interrupt requests, which can generate AOB-to-PCI interrupt request via S5933 PCIC byte#3 of AOB-to-PCI incoming mailbox #4. Refer to section 2.3, Appendix B and S5933 PCIC User's Guide for more details.

HIF_SMP0_RG, HIF_SMP1_RG HIF

Host PCI-bus interface HIF registers, which are used for selection of access mode (single- or dual-page modes) to the DPRAM/DPSEM area, of particular DPRAM or DPSEM area, and of the DPRAM memory page for host PCI-bus master access cycles to the DPRAM/DPSEM area of host PCI-bus interface. This register is available for *TORNADO-P62xx/P67* DSP systems only. Refer to section 2.3 for more details.

HM_RQ0, HM_RQ1

PCI-to-DSP interrupt requests, which are generated when host PCI-bus master writes to the *HIF_HM_RQ0_RG* and *HIF_HM_RQ1_RG* 4-bit HIF mailbox registers. Refer to sections 2.2 and 2.3 for more details.

HOST_PCIC_FIFO_RG

S5933 PCIC on-chip read-FIFO and write-FIFO PCI operation registers, which are mapped to the

PCIC area of host PCI-bus interface. Refer to section 2.3, Appendix B and S5933 PCIC User's Guide for more details.

HOST_PCIC_IMBX0_RG.. HOST_PCIC_IMBX3_RG

Read-only S5933 PCIC on-chip DSP-to-PCI Incoming Mailbox #1..#4 PCI operation registers, which are mapped to the PCIC area of host PCI-bus interface. Refer to section 2.3, Appendix B and S5933 PCIC User's Guide for more details.

HOST_PCIC_INTCSR_RG

S5933 PCIC on-chip INTCSR PCI operation register, which is mapped to the PCIC area of host PCI-bus interface. Refer to section 2.3, Appendix B and S5933 PCIC User's Guide for more details.

HOST_PCIC_MCSR_RG

S5933 PCIC on-chip MCSR PCI operation register, which is mapped to the PCIC area of host PCI-bus interface. Refer to section 2.3, Appendix B and S5933 PCIC User's Guide for more details.

HOST_PCIC_MBEF_RG

Read-only S5933 PCIC on-chip MBEF PCI operation register, which is mapped to the PCIC area of host PCI-bus interface. Refer to section 2.3, Appendix B and S5933 PCIC User's Guide for more details.

HOST_PCIC_MRAR_RG

Read-only S5933 PCIC on-chip MRAR PCI operation register, which is mapped to the PCIC area of host PCI-bus interface. This register is not available for write from the host PCI-bus interface, since PCI-bus mastering can be programmed via DSP environment only for *TORNADO-P6x* DSP systems Refer to section 2.3, Appendix B and S5933 PCIC User's Guide for more details.

HOST_PCIC_MRTC_RG

Read-only S5933 PCIC on-chip MRTC PCI operation register, which is mapped to the PCIC area of host PCI-bus interface. This register is not available for write from the host PCI-bus interface, since PCI-bus mastering can be programmed via DSP environment only for *TORNADO-P6x* DSP systems Refer to section 2.3, Appendix B and S5933 PCIC User's Guide for more details.

HOST_PCIC_MWAR_RG

Read-only S5933 PCIC on-chip MWAR PCI operation register, which is mapped to the PCIC area of host PCI-bus interface. This register is not available for write from the host PCI-bus interface, since PCI-bus mastering can be programmed via DSP environment only for *TORNADO-P6x* DSP systems Refer to section 2.3, Appendix B and S5933 PCIC User's Guide for more details.

HOST_PCIC_MWTC_RG

Read-only S5933 PCIC on-chip MWTC PCI operation register, which is mapped to the PCIC area of host PCI-bus interface. This register is not available for write from the host PCI-bus interface, since PCI-bus mastering can be programmed via DSP environment only for *TORNADO-P6x* DSP systems Refer to section 2.3, Appendix B and S5933 PCIC User's Guide for more details.

HOST_PCIC_OMBX0_RG..HOST_PCIC_OMBX3_RG

S5933 PCIC on-chip PCI-to-DSP Outgoing Mailbox #1..#4 PCI operation registers, which are mapped to the PCIC area of host PCI-bus interface. Refer to section 2.3, Appendix B and S5933

PCIC User's Guide for more details.

HPI

TMS320C6x DSP on-chip Host Port Interface, which is used for access to entire DSP environment from host PCI-bus masters. Refer to section 2.3 and to TI TMS320C6x documentation for more details.

HPI_HINT

DSP-to-PCI interrupt request via DSP on-chip HPI port (*TORNADO-P62/P67* DSP systems only). Refer to sections 2.2 and 2.3 for more details.

HPI_HPIA_RG_LSW, HPI_HPIA_RG_MSW, HPI_HPIA_RG

16-bit LSW/MSW and 32-bit DSP on-chip HPI Address Registers (*TORNADO-P62/P67* DSP systems only), which are mapped to the HPI area of host PCI-bus interface. Refer to section 2.3 and TI TMS320C6x DSP documentation for more details.

HPI_HPIC_RG_LSW, HPI_HPIC_RG_MSW, HPI_HPIC_RG

16-bit LSW/MSW and 32-bit DSP on-chip HPI Control Registers (*TORNADO-P62/P67* DSP systems only), which are mapped to the HPI area of host PCI-bus interface. Refer to section 2.3 and TI TMS320C6x DSP documentation for more details.

HPI_HPID_AINC_RG_LSW, HPI_HPID_AINC_RG_MSW, HPI_HPID_AINC_RG

16-bit LSW/MSW and 32-bit DSP on-chip HPI Data Registers with address post-increment feature (*TORNADO-P62/P67* DSP systems only), which are mapped to the HPI area of host PCI-bus interface. Refer to section 2.3 and TI TMS320C6x DSP documentation for more details.

HPI_HPID_RG_LSW, HPI_HPID_RG_MSW, HPI_HPID_RG

16-bit LSW/MSW and 32-bit DSP on-chip HPI Data Registers (*TORNADO-P62/P67* DSP systems only), which are mapped to the HPI area of host PCI-bus interface. Refer to section 2.3 and TI TMS320C6x DSP documentation for more details.

HPI32_HPIA_RG

32-bit TMS320C6202/TMS320C6203 DSP on-chip HPI Address Register (*TORNADO-P6202/P6203* DSP systems only), which is mapped to the HPI area of host PCI-bus interface. Refer to section 2.3 and TI TMS320C6x DSP documentation for more details.

HPI32_HPID_RG

32-bit TMS320C6202/TMS320C6203 DSP on-chip HPI Data Register (*TORNADO-P6202/P6203* DSP systems only), which is mapped to the HPI area of host PCI-bus interface. Refer to section 2.3 and TI TMS320C6x DSP documentation for more details.

I

IOX Area

Address area of the DSP environment, which comprise of the external DSP environment configuration registers. Refer to section 2.2 for more details.

IOX Controller

On-board DSP environment mapped hardware, which is used for DSP control. Refer to section 2.2 for more details.

J

JTAG-IN, JTAG-OUT

On-board input and output connectors, which are used for connection to external JTAG emulator and to the next device/board in JTAG path correspondingly. Refer to section 2.6 for more details.

K

L

M

MH_RQ

DSP-to-PCI interrupt request source, which is generated when DSP writes to the *DSP_MH_RQ_RG* IOX register. Refer to sections 2.2 and 2.3 for more details.

N

NMI

TMS320C6x DSP non-maskable external hardware interrupt, which are used for generation the DSP non-maskable interrupt via *DSP_NMI_SEL_RG* interrupt selector register. Refer to section 2.2 and to TI TMS320C6x documentation for more details.

nvRAM

On-board serial non-volatile memory (EEPROM or nvRAM), which is used to store start-up PCI configuration information for AMCC S5933 PCIC and to store user-defined application specific data. Refer to section 2.3, Appendix B and S5933 PCIC User's Guide for more details.

O

P

PCIC

AMCC S5933 PCI Matchmaker Controller, which is used as the interface to the PCI-bus in *TORNADO-P6x* DSP systems. Refer to sections 2.2 and 2.3, Appendix B and S5933 PCIC User's Guide for more details.

PCIC BADR-0..4

Areas of host PCI-bus interface in *TORNADO-P6x* DSP systems, which are mapped to the host PCI-bus address I/O and memory space via S5933 PCIC. Refer to section 2.3, Appendix B and S5933 PCIC User's Guide for more details.

PCI_DPRAM_IRQ

DSP-to-PCI interrupt request source via DPRAM, which is generated when host PCI-bus master writes to the DPRAM memory location *DPRAM_MH_RQ*. Refer to sections 2.2 and 2.3 for more details.

PIOX/PIOX-16

Parallel I/O eXpansion DCM site for compatible DCM. Refer to section 2.4 for more details.

Q

R

S

SBSRAM

Synchronous burst static RAM, which is a part of on-board DSP environment. Refer to section 2.2for more details.

SDRAM

Synchronous dynamic RAM, which is a part of on-board DSP environment. Refer to section 2.2 for

more details.

SIOX
Serial I/O eXpansion interface sites for compatible DCM. Refer to section 2.5 for more details.

T

TP6CC.EXE
TORNADO-P6x Control Center software utility. Refer to section 4.1 for more details.

TP6COFF.EXE
TORNADO-P6x COFF Loader software utility. Refer to section 4.2 for more details.

TSDK
TORNADO Software Development Kit software for Windows 9x/NT/2000/XP. Refer to section 4.1 for more details.

U

UTOPIA
Universal Test and Operation PHY Interface for ATM. TORNADO-P6415/P6416 DSP systems with TMS320C6415/C6416 DSP provide on-board 50 MHz 8-bit UTOPIA level 2 slave interface, which is the part of DSP on-chip peripherals. Refer to section 2.2 for more details.

V

W

WDT
Watch-dog timer, which is the part of on-board DSP environment. Refer to section 2.2 for more details.

X

XIRQ-0

External hardware DSP interrupt request from SIOX-A rev.B/C daughter-card sites, which can generate active DSP interrupt request. Refer to sections 2.2 and 2.5 for more details.

XIRQ-1

External hardware DSP interrupt request from SIOX-A rev.B and SIOX-B rev.C daughter-card sites, which can generate active DSP interrupt request. Refer to sections 2.2 and 2.5 for more details.

XIRQ-2

External hardware DSP interrupt request from SIOX-A rev.B and PIOX/PIOX-16 daughter-card sites, which can generate active DSP interrupt request. Refer to sections 2.2, 2.4 and 2.5 for more details.

XIRQ-3

External hardware DSP interrupt request from PIOX/PIOX-16 daughter-card site, which can generate active DSP interrupt request. Refer to sections 2.2 and 2.4 for more details.

Y

Z