Add-On Operation Registers 6

CONTENTS

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6.0 ADD-ON BUS OPERATION REGISTERS

The Add-On bus interface provides access to 18 DWORDs (72 bytes) of data, control and status information. All of these locations are accessed by asserting the Add-On bus chip select pin (SELECT#) in conjunction with either the read or write control strobes (signal pin RD# or WR#). Access to the FIFO can also be achieved through use of the dedicated pins, RDFIFO# and WRFIFO#. The dedicated pins for control of the FIFO are provided to optionally implement Direct Memory Access (DMA) on the Add-On bus, or to connect with an external FIFO.

This register group represents the primary method for communication between the Add-On and PCI buses as viewed by the Add-On. The flexibility of this arrangement allows a number of user-defined software protocols to be built. For example, data, software assigned commands, and command parameters can be exchanged between the PCI and Add-On buses using either the mailboxes or FIFOs with or without handshaking interrupts. The register structure is very similar to that of the PCI operation register set. The major difference between the PCI bus and Add-On bus register complement are the absence of bus master control registers (4) on the Add-On side and the addition of two “pass-through” registers. Table 6-1 lists the Add-On interface registers.

Table 6-1. Operation Registers — Add-On Interface

Address	Abbreviation	Register Name
00h	AIMB1	Add-On Incoming Mailbox Register #1
04h	AIMB2	Add-On Incoming Mailbox Register #2
08h	AIMB3	Add-On Incoming Mailbox Register #3
0Ch	AIMB4	Add-On Incoming Mailbox Register #4
10h	AOMB1	Add-On Outgoing Mailbox Register #1
14h	AOMB2	Add-On Outgoing Mailbox Register #2
18h	AOMB3	Add-On Outgoing Mailbox Register #3
1Ch	AOMB4	Add-On Outgoing Mailbox Register #4
20h	AFIFO	Add-On FIFO port
24h	MWAR [1]	Bus Master Write Address Register
28h	APTA	Add-On Pass-Through Address
2Ch	APTD	Add-On Pass-Through Data
30h	MRAR [1]	Bus Master Read Address Register
34h	AMBEF	Add-On Mailbox Empty/Full Status
38h	AINT	Add-On Interrupt control
3Ch	AGCSTS	Add-On General Control and Status Register
58h	MWTC [1]	Bus Master Write Transfer Count
5Ch	MRTC [1]	Bus Master Read Transfer Count

Note 1: See Section 10.1.4.1 for PCI Bus Master Control from the Add-On interface.

6.1 ADD-ON INCOMING MAILBOX REGISTERS (AIMBx)

Register Names: Add-On Incoming Mailboxes 1-4

Add-On Address Offset: 00h, 04h, 08h, 0Ch

Power-up value: XXXXXXXXh

Attribute: Read Only

Size: 32 bits

These four DWORD registers provide a method for receiving data, commands, or command parameters from the PCI interface. Add-On read operations to these registers may be in any width (byte, word, or DWORD). These registers are read-only. Writes to this address space have no effect. Reading from one of these registers can optionally cause a PCI bus interrupt (if desired) when the PCI interrupt control/ status register (Section 5.9) is properly configured.

6.2 ADD-ON OUTGOING MAILBOX REGISTERS (AOMBx)

Register Names: Add-On Outgoing Mailboxes 1-4

Add-On Address Offset: 10h, 14h, 18h, 1Ch

Power-up value: XXXXXXXXh

Attribute: Read/Write

Size: 32 bits

These four DWORD registers provide a method for sending data, commands, or command parameters or status to the PCI interface. Add-On write operations to these registers may be in any width (byte, word, or DWORD). These registers may also be read. Writing to one of these registers can optionally cause a PCI bus interrupt (if desired) when the PCI interrupt control/status register (Section 5.9) is properly configured.

Mailbox 4, byte 3 only exists as device pins on the S5933 device when used with a serial nonvolatile memory. This byte is not available if a byte-wide nv memory is used.

6.3 ADD-ON FIFO REGISTER PORT (AFIFO)

Register Name: Add-On FIFO Port

Add-On Address Offset: 20h

Power-up value: XXXXXXXXh

Attribute: Read/Write

Size: 32 bits

This location provides access to the bidirectional FIFO. Separate registers are involved when reading and writing to this location. Accordingly, it is not possible to read what was written to this location. The sequence of filling and emptying this FIFO is established by the PCI interface interrupt control and Status Register (Section 5.9).

The FIFO's fullness may be observed by reading the master control/status register, AGCSTS, described in Section 5.8. Additionally, two signal pins are provided which reveal whether data is available (RDEMPTY) or space to write into the FIFO is available (WRFULL). These signals may be used to interface with user supplied DMA logic. Caution must be exercised when using these flags for FIFO transfers involving 64 bit endian conversion since the FIFO must operate on DWORD pairs.

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6.4 ADD-ON CONTROLLED BUS MASTER WRITE ADDRESS REGISTER (MWAR)

Register Name: Master Write Address
Add-On Address Offset: 24h
Power-up value: 00000000h
Attribute: Read/Write
Size: 32 bits

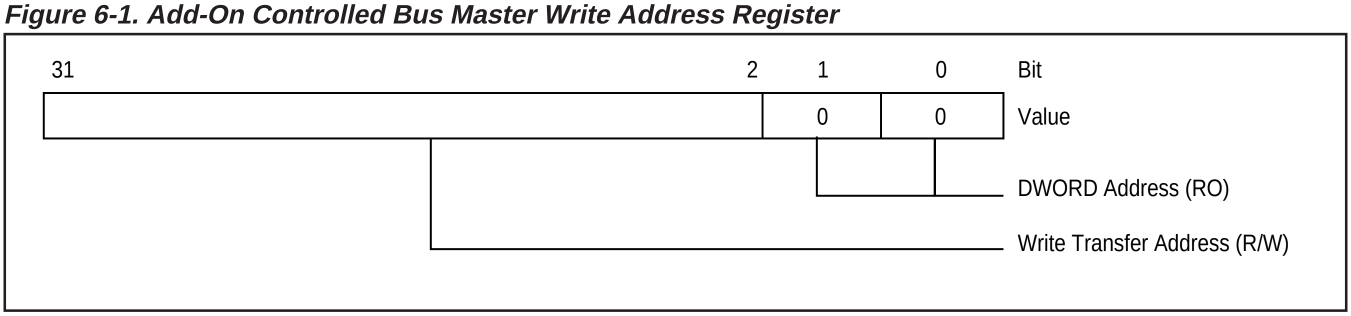
This register is only accessible when Add-On initiated bus mastering is enabled. See Section 11.2.3.3.

This register is used to establish the PCI address for data moving from the Add-On bus to the PCI bus during PCI bus memory write operations. It consists of a 30-bit counter with the low-order two bits hardwired as zeros. Transfers may be any non-zero byte length as defined by the transfer count register, MWTC (Section 6.11), and must begin on a DWORD boundary. This DWORD boundary starting constraint is placed upon this controller's PCI bus master transfers so that byte lane alignment can be maintained between the S5933 controller's internal FIFO data path, the Add-On interface, and the PCI bus.

Note: Applications which require a non-DWORD starting boundary will need to move the first few bytes under software program control (and without using the FIFO) to establish a DWORD boundary. After the DWORD boundary is established the S5933 can begin the task of PCI bus master data transfers.

The Master Write Address Register is continually updated during the transfer process and will always be pointing to the next unwritten location. Reading of this register during a transfer process (done when the S5933 controller is functioning as a target, i.e. not a bus master) is permitted and may be used to monitor the progress of the transfer. During the address phase for bus master write transfers, the two least significant bits presented on the PCI bus pins AD[31:0] will always be zero. This identifies to the target memory that the burst address sequence will be in a linear order rather than in an Intel 486 or Pentium™ cache line fill sequence. Also, the PCI bus address bit A1 will always be zero when this controller is the bus master. This signifies to the target that the S5933 controller is burst capable and that the target should not arbitrarily disconnect after the first data phase of this operation.

Figure 6-1. Add-On Controlled Bus Master Write Address Register



6.5 ADD-ON PASS-THRU ADDRESS REGISTER (APTA)

Register Name:	Add-On Pass-Thru Address
Add-On Address Offset:	28h
Power-up value:	XXXXXXXXh
Attribute:	Read Only
Size:	32 bits

This register is employed when a response is desired when one of the Base address decode regions (see Section 3.11) is selected during an active PCI bus cycle. When one of the base address decode registers 1-4 encounters a PCI bus cycle which selects the region defined by it, this device latches that current cycle's active address and asserts the signal PTATN# (Pass-Thru ATtentioN). Wait states are generated on the PCI bus until either data is transferred or the PCI bus cycle is aborted by the initiator. (See Section 12.2)

This register provides a method for “live” data (registered) transfers. Intended uses include the emulating of other hardware as well as enabling the connection of existing external hardware to interface to the PCI bus through the S5933.

6.6 ADD-ON PASS-THRU DATA REGISTER (APTD)

Register Name:	Add-On Pass-Thru Data
Add-On Address Offset:	2Ch
Power-up value:	XXXXXXXXh
Attribute:	Read/Write
Size:	32 bits

This register, along with APTA described above, is employed when a response is desired should one of the Base address decode regions become selected during an active PCI bus cycle (see Section 4.11). When one of the base address decode registers 1-4 encounters a PCI bus cycle which selects the region defined by it, the APTA register will contain that current cycle's active address and the device asserts the signal PTATN# (Pass-Thru ATentioN). Wait states are generated on the PCI bus until this register is read (PCI bus writes) or this register is written (PCI bus reads).

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6.7 ADD-ON CONTROLLED BUS MASTER READ ADDRESS REGISTER (MRAR)

Register Name: Master Read Address
Add-On Address Offset: 30h
Power-up value: 00000000h
Attribute: Read/Write
Size: 32 bits

This register is only accessible when Add-On initiated bus mastering is enabled. See Section 11.2.3.3.

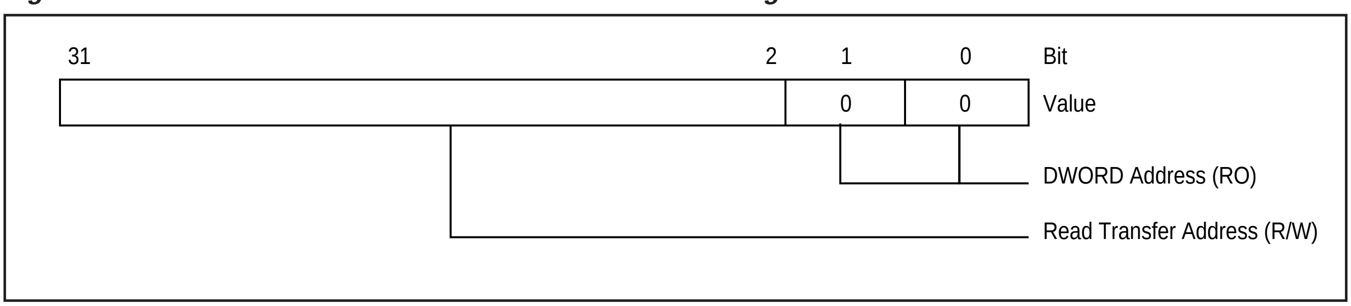
This register is used to establish the PCI address for data moving to the Add-On bus from the PCI bus during PCI bus memory read operations. It consists of a 30-bit counter with the low-order two bits hardwired as zeros. Transfers may be any non-zero byte length as defined by the transfer count register, MRTC (Section 5.7) and must begin on a DWORD boundary. This DWORD boundary starting constraint is placed upon this controller's PCI bus master transfers so that byte lane alignment can be maintained between the S5395X controller's internal FIFO data path, the Add-On interface and the PCI bus.

Note: Applications which require a non-DWORD starting boundary will need to move the first few bytes under software program control (and without using the FIFO) to establish a DWORD boundary. After the DWORD boundary is established the S5933 can begin the task of PCI bus master data transfers.

The Master Read Address Register is continually updated during the transfer process and will always be pointing to the next unread location. Reading of this register during a transfer process (done when the S5933 controller is functioning as a target—i.e., not a bus master) is permitted and may be used to monitor the progress of the transfer. During the address phase for bus master read transfers, the two least significant bits presented on the PCI bus AD[31:0] will always be zero. This identifies to the target memory that the burst address sequence will be in a linear order rather than in an Intel 486 or Pentium™ cache line fill sequence. Also, the PCI bus address bit A1 will always be zero when this controller is the bus master. This signifies to the target that the controller is burst capable and that the target should not arbitrarily disconnect after the first data phase of this operation.

Under certain circumstances, MRAR can be accessed from the Add-On bus instead of the PCI bus. See Section 11.1.4.1.

Figure 6-2. Add-On Controlled Bus Master Read Address Register



6.8 ADD-ON EMPTY/FULL STATUS REGISTER (AMBEF)

Register Name: Add-On Mailbox Empty/Full Status

Add-On Address Offset: 34h

Power-up value: 00000000h

Attribute: Read Only

Size: 32 bits

This register provides empty/full visibility of each byte within the mailboxes. The empty/full status for the Outgoing mailboxes are displayed on the high order 16 bits and the empty/full status for the incoming mailboxes are presented on the low order 16 bits. A value of one signifies that a given mailbox had been written by the sourcing interface but had not yet been read by the corresponding destination interface. An incoming mailbox is defined as one in which data travels from the PCI bus into the Add-On bus and an outgoing mailbox is defined as one where data goes OUT from the Add-On bus to the PCI interface.

Figure 6-3. Add-On Mailbox Empty/Full Status Register

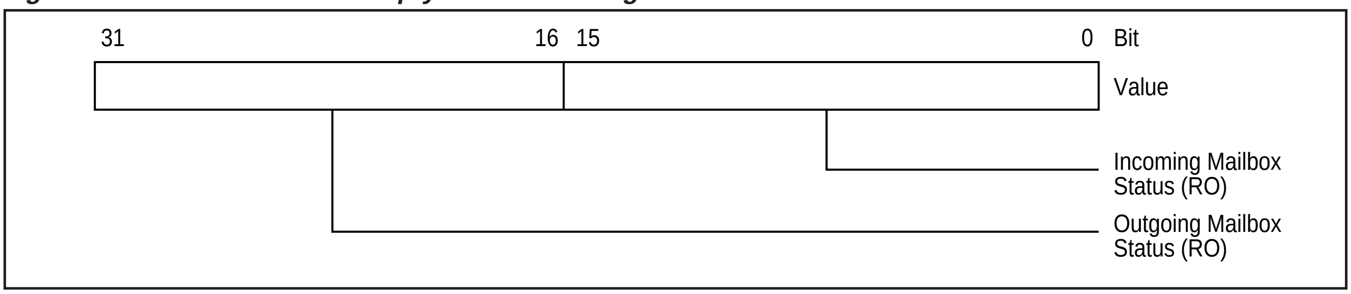


Table 6-2. Add-On Mailbox Empty/Full Status Register

Bit	Description
31:16	Outgoing Mailbox Status. This field indicates which outgoing mailbox registers have been written by the Add-On bus interface but have not yet been read by the PCI bus. Each bit location corresponds to a specific byte within one of the four outgoing mailboxes. A value of one for each bit signifies that the specified mailbox byte is full, a value of zero signifies empty. The mapping of these status bits to bytes within each mailbox is as follows: Bit 31 = Outgoing mailbox 4 byte 3 Bit 30 = Outgoing mailbox 4 byte 2 Bit 29 = Outgoing mailbox 4 byte 1 Bit 28 = Outgoing mailbox 4 byte 0 Bit 27 = Outgoing mailbox 3 byte 3 Bit 26 = Outgoing mailbox 3 byte 2 Bit 25 = Outgoing mailbox 3 byte 1 Bit 24 = Outgoing mailbox 3 byte 0 Bit 23 = Outgoing mailbox 2 byte 3 Bit 22 = Outgoing mailbox 2 byte 2 Bit 21 = Outgoing mailbox 2 byte 1 Bit 20 = Outgoing mailbox 2 byte 0 Bit 19 = Outgoing mailbox 1 byte 3 Bit 18 = Outgoing mailbox 1 byte 2 Bit 17 = Outgoing mailbox 1 byte 1 Bit 16 = Outgoing mailbox 1 byte 0
15:00	Incoming Mailbox Status. This field indicates which incoming mailbox registers have been written by the PCI bus but not yet been read by the Add-On interface. Each bit location corresponds to a specific byte within one of the four incoming mailboxes. A value of one for each bit signifies that the specified mailbox byte is full, a value of zero signifies empty. The mapping of these status bits to bytes within each mailbox is as follows: Bit 15 = Incoming mailbox 4 byte 3 Bit 14 = Incoming mailbox 4 byte 2 Bit 13 = Incoming mailbox 4 byte 1 Bit 12 = Incoming mailbox 4 byte 0 Bit 11 = Incoming mailbox 3 byte 3 Bit 10 = Incoming mailbox 3 byte 2 Bit 9 = Incoming mailbox 3 byte 1 Bit 8 = Incoming mailbox 3 byte 0 Bit 7 = Incoming mailbox 2 byte 3 Bit 6 = Incoming mailbox 2 byte 2 Bit 5 = Incoming mailbox 2 byte 1 Bit 4 = Incoming mailbox 2 byte 0 Bit 3 = Incoming mailbox 1 byte 3 Bit 2 = Incoming mailbox 1 byte 2 Bit 1 = Incoming mailbox 1 byte 1 Bit 0 = Incoming mailbox 1 byte 0

6.9 ADD-ON INTERRUPT CONTROL/ STATUS REGISTER (AINT)

Register Name:	Add-On Interrupt Control and Status
Add-On Address Offset:	38h
Power-up value:	00000000h
Attribute:	Read/Write, Read/Write_One_Clear
Size:	32 bits

This register provides the method for choosing which conditions are to produce an interrupt on the Add-On bus interface, a method for viewing the cause for the interrupt, and a method for acknowledging (removing) the interrupt's assertion.

Interrupt sources:

- One of the Incoming mailboxes (1,2,3 or 4) becomes full.
- One of the Outgoing mailboxes (1,2,3 or 4) becomes empty.
- Built-in self test issued.
- Write Transfer Count = zero
- Read Transfer Count = zero
- Target/Master Abort

Figure 6-4. Add-On Interrupt Control/Status Register

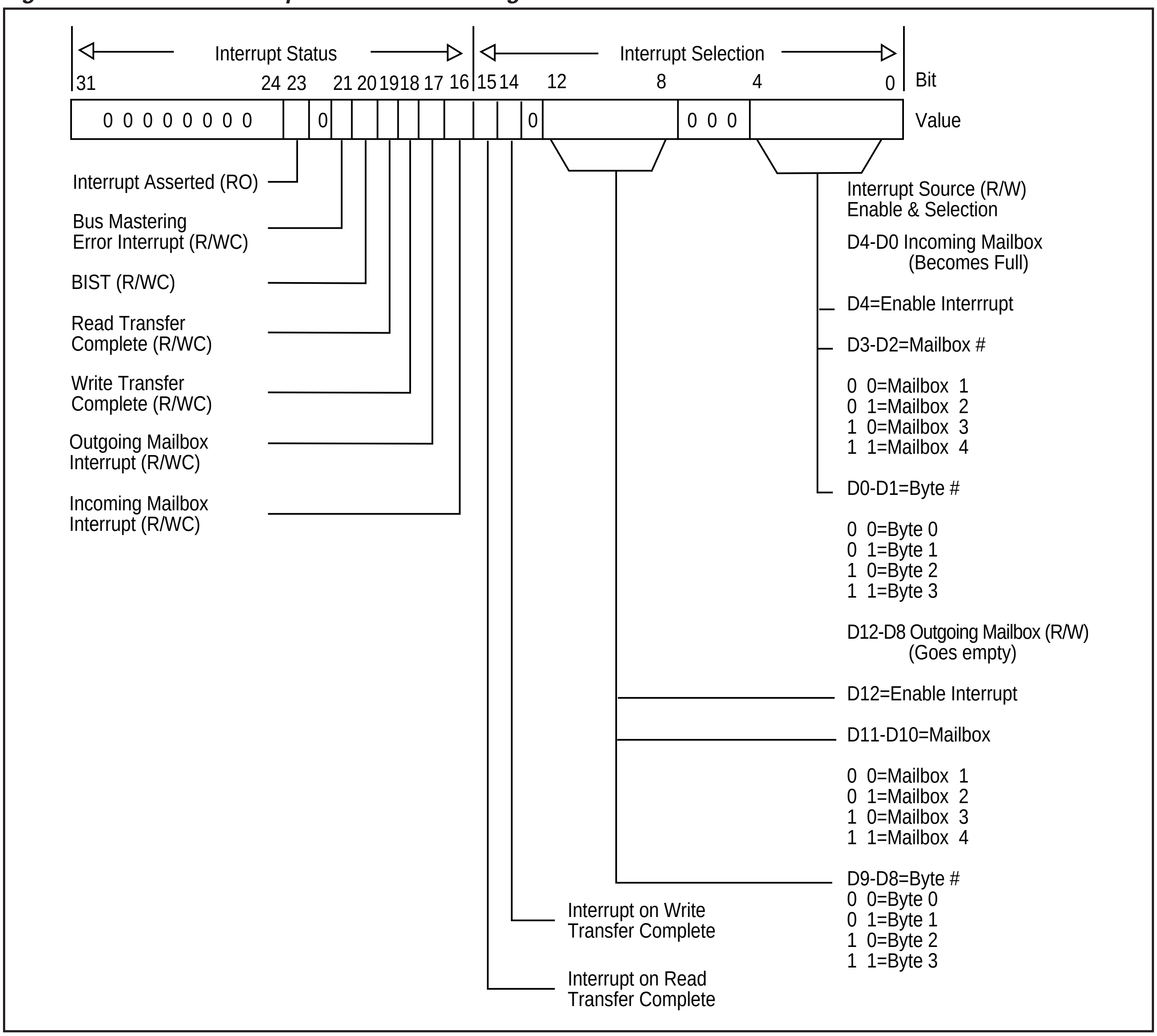


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Table 6-3. Interrupt Control/Status Register

Bit	Description
31:24	Reserved. Always zero.
23	Interrupt asserted. This read-only status bit indicates that one or more interrupt conditions is present. This bit is nothing more than the ORing of the interrupt conditions described by bits, 20, 17 and 16 of this register.
22	Reserved. Always zero.
21	Master/Target Abort. This bit signifies that an interrupt has been generated due to the S5933 encountering a Master or Target abort during an S5933 initiated PCI bus cycle. This bit operates as read or write one clear. Writing a one to this bit causes it to be cleared. Writing a zero to this bit does nothing.
20	BIST. Built-In Self-Test interrupt. This interrupt occurs when a self test is initiated by the PCI interface writing of the BIST configuration register (Section 4.10). This bit will stay set until cleared by writing a one to this location. Self test completion codes may be passed to the PCI BIST register by writing to the AGCSTS register described in Section 6.10.
19	Read Transfer Complete. This bit signifies that an interrupt has been generated due to the completion of a PCI bus master operation involving the transfer of data from the PCI bus to the Add-On. This interrupt will occur when the Master Read Transfer Count register reaches zero. This bit operates as read or write one clear. A write to this bit with the data of one will cause this bit to be reset; a write to this bit with the data of zero will not change the state of this bit.
18	Write Transfer Complete. This bit signifies that an interrupt has been generated due to the completion of a PCI bus master operation involving the transfer of data to the PCI bus from the Add-On. This interrupt will occur when the Master Write Transfer Count register reaches zero. This bit operates as read or write one clear. A write to this bit with the data of one will cause this bit to be reset; a write to this bit with the data of zero will not change the state of this bit.
17	Outgoing Mailbox Interrupt. This bit sets when the mailbox selected by bits 12 through 8 of this register is read by the PCI interface. This bit operates as read or write one clear. A write to this bit with the data as one will cause this bit to be reset; a write to this bit with the data as zero will not change the state of this bit.
16	Incoming Mailbox Interrupt. This bit sets when the mailbox selected by bits 5 through 0 of this register are written by the PCI interface. This bit operates as read or write one clear. A write to this bit with the data of one will cause this bit to be reset; a write to this bit with the data as zero will not change the state of this bit.
15	Interrupt on Read Transfer Complete. This bit enables the occurrence of an interrupt when the read transfer count reaches zero. This bit is read/write.
14	Interrupt on Write Transfer Complete. This bit enables the occurrence of an interrupt when the write transfer count reaches zero. This bit is read/write.
13	Reserved. Always zero.
12	Enable outgoing mailbox interrupt. This bit allows a read by the PCI of the outgoing mailbox register identified by bits 11 through 8 to produce an Add-On interface interrupt. This bit is read/write.
11:10	Outgoing Mailbox Interrupt Select. This field selects which of the four outgoing mailboxes is to be the source for causing an outgoing mailbox interrupt. [00]b selects mailbox 1, [01]b selects mailbox 2, [10]b selects mailbox 3 and [11]b selects mailbox 4. This field is read/write.
9:8	Outgoing Mailbox Byte Interrupt select. This field selects which byte of the mailbox selected by bits 11 and 10 above is to actually cause the interrupt. [00]b selects byte 0, [01]b selects byte 1, [10]b selects byte 2, and [11]b selects byte 3. This field is read/write.
7:5	Reserved. Always zero.

Table 6-3. Interrupt Control/Status Register (Continued)

Bit	Description
4	Enable incoming mailbox interrupt. This bit allows a write from the PCI bus to the incoming mailbox register identified by bits 3 through 0 to produce an Add-On interface interrupt. This bit is read/write.
3:2	Incoming Mailbox Interrupt Select. This field selects which of the four incoming mailboxes is to be the source for causing an incoming mailbox interrupt. [00]b selects mailbox 1, [01]b selects mailbox 2, [10]b selects mailbox 3 and [11]b selects mailbox 4. This field is read/write.
1:0	Incoming Mailbox Byte Interrupt select. This field selects which byte of the mailbox selected by bits 3 and 2 above is to actually cause the interrupt. [00]b selects byte 0, [01]b selects byte 2, and so on.

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6.10 ADD-ON GENERAL CONTROL/STATUS REGISTER (AGCSTS)

Register Name: Add-On General Control and Status

Add-On Address Offset: 3Ch

Power-up value: 000000F4h (PCI initiated bus mastering) 00000034h (Add-On initiated bus mastering)

Attribute: Read/Write, Read Only, Write Only

Size: 32 bits

This register provides for overall control of the Add-On portion of this device. It is used to provide a method to perform software resets of the mailbox and FIFO flags.

The following Add-On controls are provided:

- Reset PCI to Add-On FIFO flags
- Reset Add-On to PCI FIFO flags
- Reset mailbox empty full status flags
- Write/read external non-volatile memory.

The following status flags are provided to the Add-On:

- Add-On to PCI FIFO FULL
- Add-On to PCI FIFO has four or more empty locations
- Add-On to PCI FIFO EMPTY
- PCI to Add-On FIFO FULL
- PCI to Add-On FIFO has four or more words loaded
- PCI to Add-On FIFO EMPTY

Figure 6-5. Add-On General Control/Status Register

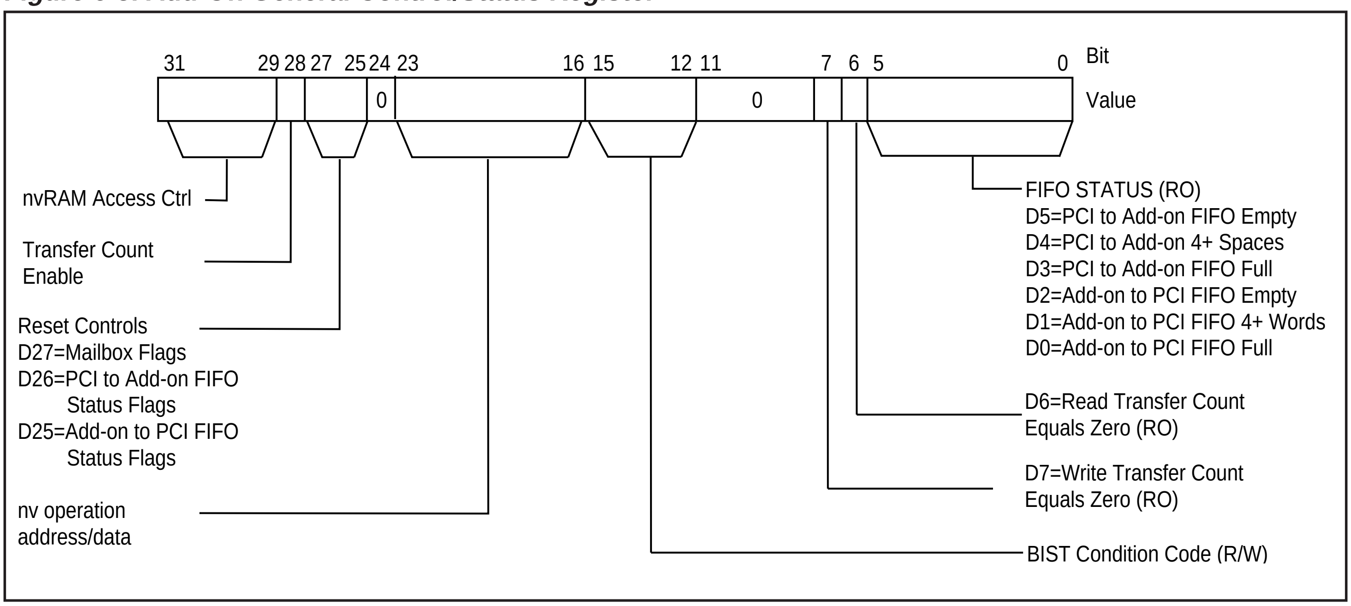

Table 6-4. Add-On General Control/Status Register

Bit	Description
31:29	nvRAM/EPROM Access Control. This field provides a method for access to the optional, external non-volatile memory. Write operations are achieved by a sequence of byte operations involving these bits and the 8-bit field of bits 23 through 16. The sequence requires that the low-order address, high-order address, and then a data byte be loaded in order. Bit 31 of this field acts as an enable/clock and ready for the access to the external memory. D31 must be written to a 1 before an access can begin, and subsequent accesses must wait for bit D31 to become zero (ready). D31 D30 D29 W/R 0 X X W Inactive 1 0 0 W Load low address byte 1 0 1 W Load high address byte 1 1 0 W Begin write 1 1 1 W Begin read 0 X X R Ready 1 X X R Busy Cautionary note: The non-volatile memory interface is also available for access by the PCI bus interface. Accesses by both the Add-On and PCI bus to the nv memory are not directly supported by this component. Software must be designed to prevent the simultaneous access of nv memory to prevent data corruption within the memory and provide for accurate data retrieval.
28	Transfer Count Enable. When set, transfer counts are used for Add-On initiated bus master transfers. When clear, transfer counts are ignored.
27	Mailbox Flag Reset. Writing a 1 to this bit causes all mailbox status flags to become reset (EMPTY). It is not necessary to write this bit as 0 because it is used internally to produce a reset pulse. Since reading of this bit will always produce zeros, this bit is write only.
26	PCI to Add-On FIFO Status Reset. Writing a 1 to this bit causes the Inbound (Bus master reads) FIFO empty flag to set indicating empty and the FIFO FULL flag to reset and the FIFO Four Plus spaces flag to set. It is not necessary to write this bit as 0 because it is used internally to produce a reset pulse. Since reading of this bit would always produce zeros, this bit is write only.
25	Add-On to PCI FIFO Status Reset. Writing a one to this bit causes the Outbound (Bus master writes) FIFO empty flag to set indicating empty and the FIFO FULL flag to reset and the FIFO Four Plus words available flag to reset. It is not necessary to write this bit as zero because it is used internally to produce a reset pulse. Since reading of this bit would always produce zeros, this bit is write only.
24	Reserved. Always zero.
23:16	Non-volatile memory address/data port. This 8-bit field is used in conjunction with bit 31, 30 and 29 of this register to access the external non-volatile memory. The contents written are either low address, high address, or data as defined by bits 30 and 29. This register will contain the external non-volatile memory data when the proper read sequence for bits 31 through 29 is performed.
15:12	BIST condition code. This field is directly connected to the PCI configuration self test register described in Section 4.10. Bit 15 through 12 maps with the BIST register bits 3 through 0, respectively.
11:8	Reserved. Always zero.

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Table 6-4. Add-On General Control/Status Register (Continued)

Bit	Description
7	Add-On to PCI Transfer Count Equal Zero (RO). This bit as a one signifies that the write transfer count is all zeros. Only when Add-On initiated bus mastering is enabled.
6	PCI to Add-On Transfer Count Equals Zero (RO). This bit as a one signifies that the read transfer count is all zeros. Only when Add-On initiated bus mastering is enabled.
5	PCI to Add-On FIFO Empty. This bit is a 1 when the PCI to Add-On FIFO is empty.
4	PCI to Add-On FIFO 4+ spaces. This bit is a 1 when there are four or more open spaces in the PCI to Add-On FIFO.
3	PCI to Add-On FIFO Full. This bit is a 1 when the PCI to Add-On FIFO is full.
2	Add-On to PCI FIFO Empty. This bit is a 1 when the Add-On to PCI FIFO is empty.
1	Add-On PCI FIFO 4+ words. This bit is a 1 when there are four or more full locations in the Add-On to PCI FIFO.
0	Add-On to PCI FIFO Full. This bit is a 1 when the Add-On to PCI FIFO is full.

6.11 ADD-ON CONTROLLED BUS MASTER WRITE TRANSFER COUNT REGISTER (MWTC)

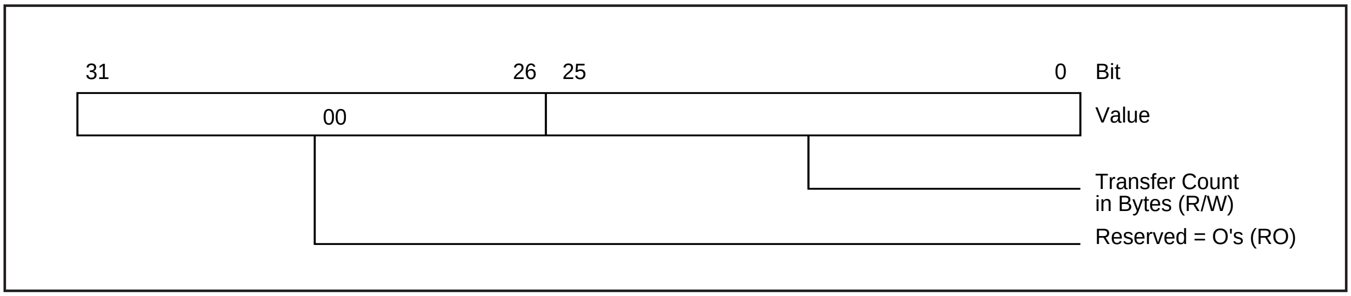
Register Name: Master Write Transfer Count
Add-On Address Offset: 58h
Power-up value: 00000000h
Attribute: Read/Write
Size: 32 bits

This register is only accessible when Add-On initiated bus mastering is enabled. See Section 11.2.3.3.

The master write transfer count register is used to convey to the S5933 controller the actual number of bytes that are to be transferred. The value in this register is decremented with each bus master PCI write operation until the transfer count reaches zero.

Upon reaching zero, the transfer operation ceases and an interrupt may be optionally generated to either the PCI or Add-On bus interface. Transfers which are not whole multiples of DWORDs in size result in a partial word ending cycle. This partial word ending cycle is possible since all bus master transfers for this controller are required to begin on a DWORD boundary.

Figure 6-6. Add-On Controlled Bus Master Write Transfer Count Register



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6.12 ADD-ON CONTROLLED BUS MASTER READ TRANSFER COUNT REGISTER (MRTC)

Register Name: Master Read Transfer Count
Add-On Address Offset: 5Ch
Power-up value: 00000000h
Attribute: Read/Write
Size: 32 bits

This register is only accessible when Add-On initiated bus mastering is enabled. See Section 11.2.3.3.

The master read transfer count register is used to convey to the PCI controller the actual number of bytes that are to be transferred. The value in this register is decremented with each bus master PCI read operation until the transfer count reaches zero. Upon reaching zero, the transfer operation ceases and an interrupt may be optionally generated to either the PCI or Add-On bus interface. Transfers which are not whole multiples of DWORDs in size result in a partial word ending cycle. This partial word ending cycle is possible since all bus master transfers for this controller are required to begin on a DWORD boundary.

Figure 6-7. Add-On Controlled Bus Master Read Transfer Count Register